Transport and Noise Properties of Nanostructure Transistors for Biosensor Applications

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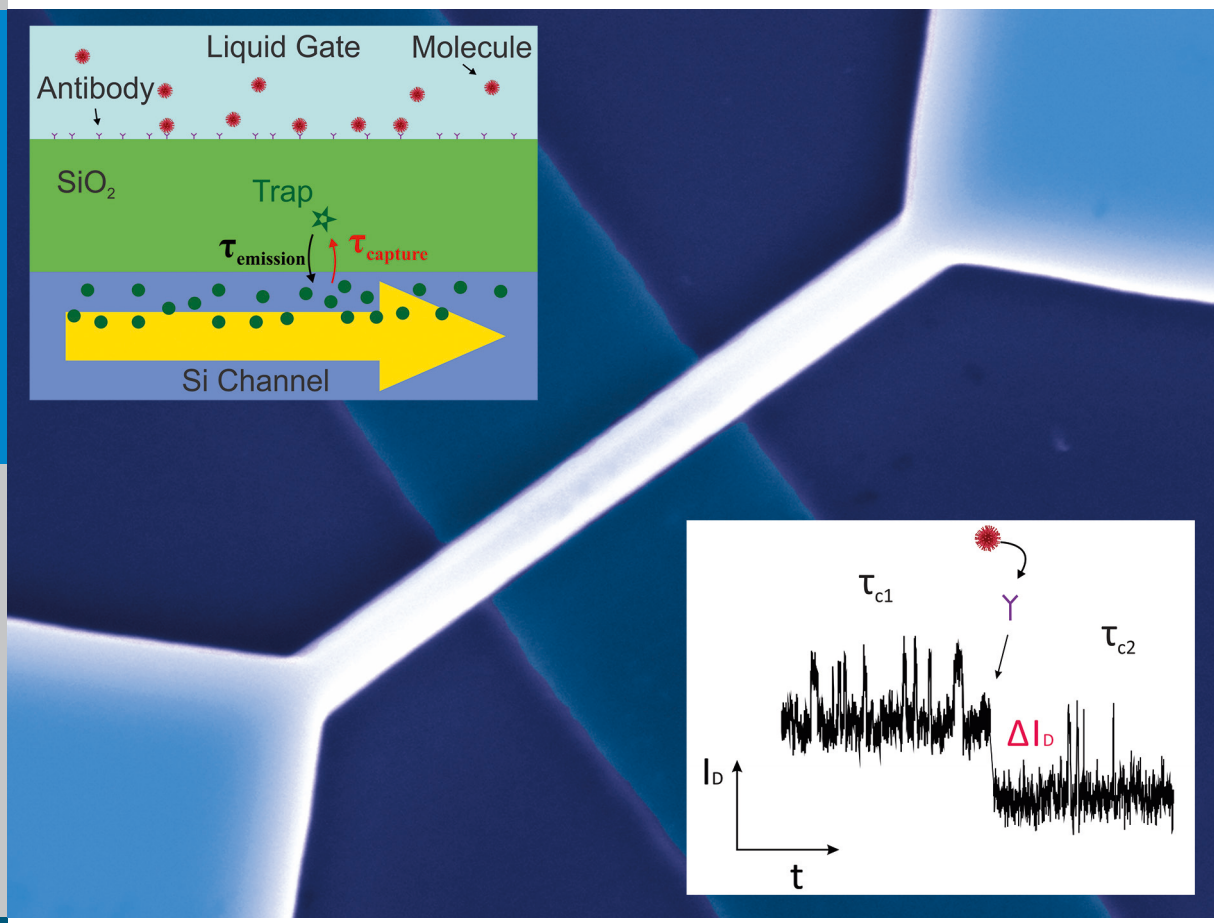

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Science is not only the science itself, it includes the life, to be honest, to be decent!

Abstract

Biosensors based on nano-scale electronic devices have the potential to achieve exquisite sensitivity for the direct detection of biomolecular interactions. Silicon nanowire field effect transistors (Si NW FET) are the most promising candidates for these purposes because of their biocompatibility, very high surface-to-volume ratio, fast response, and good reliability of the signal. In the last decade, several promising results based on Si NW sensors, which were either fabricated by “top-down” or “bottom-up” approaches, have been reported.

However, a fundamental understanding of the principle determining the signal-to-noise ratio (SNR) of the Si NW FET biosensors is still not well understood.

The aim of this PhD thesis was to fabricate Si NW FETs with optimized techniques based on the “top-down” approach and to study the electrical transport characteristics of Si NW FETs with different channel dimensions in order to disclose the intrinsic low frequency noise properties and hence give the inspiration for biosensor fabrication and application.

Nanoimprint lithography (NIL) and wet anisotropic etching were employed in the fabrication of our devices. In order to increase the size resolution, reproducibility and stable electrical operation properties, KOH chemical etching was used to fabricate imprint mold.

Four kinds of Si NW FETs were fabricated using the optimized CMOS compatible technologies in the cleanroom of the Helmholtz Nanoelectronic Facility (HNF), Forschungszentrum Juelich, Germany.

The electrical transport properties of Si NW FETs were characterized by both current-voltage characteristics and low frequency noise measurements using different configurations, including back gate control (V_{BG}) and front gate control (V_{FG}) in ambient conditions and in liquid environments, respectively. It was demonstrated that the magnitude of the flicker noise depends on the channel dimensions and that the signal to noise ratio increases with the shrinking of the channel dimensions. Furthermore, random telegraph signals (RTSs) were registered in devices with short channels and Coulomb Blockade energy was evaluated from the real time and low frequency noise measurements at different temperatures in a back gate configuration. RTS noise was also found in the front gate configuration at different pH values and different gate voltages. It was demonstrated that the capture time constant of the RTS can be used as a sensor analysis with a higher sensitivity of signal detection in sensor applications than conventional drain current measurements and the sensitivity can be further improved by a special design of the structures.

Zusammenfassung

Auf Nanoelektronik basierende Biosensoren können biomolekulare Vorgänge mit hoher Empfindlichkeit nachweisen. Der vielversprechendste Sensor im Hinblick auf Eigenschaften wie Bio-Kompatibilität, einem hohen Verhältnis zwischen der Oberfläche und dem Volumen, Schnelligkeit und Zuverlässigkeit, ist der Silizium-Nanodraht-Feldeffekt-Transistor (SiNW-FET „Silicon nanowire field effect transistor“). In den letzten Jahren haben sowohl „bottom-up“ als auch „top-down“ Ansätze zu guten Resultaten geführt.

Dennoch sind die entscheidenden Effekte, welche das Signal-Rausch Verhältnis dieser BioFETs bestimmen, noch nicht vollkommen verstanden.

Das Ziel dieser Arbeit war es den „top-down“ Ansatz zu nutzen um SiNW FETs herzustellen und zu optimieren, sowie die elektrischen Transporteigenschaften der „Silicium Nanodraht FETs“ bezüglich verschiedener Kanalgrößen zu untersuchen. Dies erlaubt die intrinsischen Tieffrequenz-Eigenschaften zu verstehen und die Herstellung der Sensoren zu optimieren.

Die Herstellung der Proben wurde mit lithographischem Nanoimprint-Verfahren und anisotropem Ätzen durchgeführt. Außerdem wurde Nassätzen mit KOH benutzt um die Auflösung und Reproduzierbarkeit, sowie die Stabilität der Proben zu erhöhen.

Vier verschiedene Arten von Si-Nanodrähten wurden im Reinraum der „Helmholtz Nanoelectronic Facility“ im Forschungszentrum Jülich, Deutschland, mit optimiertem, CMOS-kompatiblem Verfahren hergestellt.

Durch Strom-Spannungskurven-Kurven und Tieffrequenz-Rauschmessungen wurden die elektrischen Transporteigenschaften untersucht. Dabei wurde das elektrische Verhalten des SiNW FETs durch Rückseiten-Steuerelektroden („back-gate“) und Vorderseiten-Steuerelektroden („front-gate“) in gasförmiger und flüssiger Umgebung kontrolliert.

Diese Messungen zeigen, dass die Größenordnung des „Flicker“-Rauschens von der Größe des Kanals abhängt, und dass die Empfindlichkeit mit zunehmender Verkleinerung des Kanals steigt. In Proben mit kurzen Kanälen wurden „Random telegraph“- Signale (RTS) registriert.

Die Position und Energie im Regime der Coulomb-Blockade wurde aus Messungen im „back-gate“-Betrieb bei verschiedenen Temperaturen bestimmt. Auch im „front-gate“-Betrieb wurde das RTS-Rauschen bei verschiedenen pH-Werten und angelegten Spannungen gemessen. Dabei wurde gezeigt, dassstatt der üblichen Leitfähigkeitsmessungen die Erfassungszeit der RTS als Parameter genutzt werden kann um die Empfindlichkeit der Signalerfassung zu steigern.

Acknowledgements

I would like to express my sincere gratitude to my advisors, collaborators, as well as to my family and friends who have supported me during my PhD.

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Contents

1. Introduction

1.1 Motivation

The first experimental fabrication of the junction gate field effect transistor (JFET) [1] in 1947 gave rise to the new era of semiconductor electronics. The metal oxide semiconductor field effect transistor (MOSFET) was proposed in 1961 [1, 2] and has largely superseded the JFET. It has become the dominant electronic device, and without a doubt continues to play a key role in the modern electronic world. During the last 60 years, the continuous downscaling of electronic devices followed Moore's law [3]. Geometric scaling of transistor dimensions has been the main driver for further improvement of the device operation speed and simultaneously has decreased the cost per transistor. Today, state of the art MOSFETs have effective gate lengths of only a few tens of nanometers, pushing the conventional MOSFET electronics towards nanoelectronics and quantum electronics.

Recently, the interdisciplinary studies [4, 5], which integrating knowledge including nanelectronics, biology, chemistry and medicine to develop advanced devices based bio/chemical system, have attracted a lot of researchers' attention. The similarity in sizes of synthetic and natural nanostructures makes nanotechnology an obvious choice for identification and quantification of biological and chemical species, which are central issues in modern medical and biochemical applications, ranging from diagnosing disease to discovery and screening of new drug molecules [6]. Nano objects, such as nanowires [7, 8] and carbon nanotubes [9] as well as nanoparticles[10], offer new and sometimes unique opportunities for these key tasks.

Semiconductor nanowires are structures scaled down to tens of nanometers in width, representing pseudo-one-dimensional structures with relatively long length, typically in the range of micrometers to several hundred nanometers. In 2001, Lieber's group reported the first utilization of silicon nanowires (Si NW) for biological and chemical sensor applications [8]. Since then, enormous research efforts to design and develop high performance NW based sensors have been done. Owing to the extremely large surface-to-volume ratio of one dimensional nanostructures, it is possible to develop sensors with exquisite sensitivity [11]. Any small disturbance of the NW surface potential, such as the adsorption of charged molecules on the surface, may result in a large change in electrical conductance. Silicon nanowire field effect transistors (Si NW FETs) are emerging as a powerful approach for label-free, ultrasensitive and highly-selective real-time detection of biological, chemical species and cellular signal investigation [8, 12], including proteins [13, 14], nucleic acids [15], viruses [16] as well as biochemical signaling events such as cells or neuronal action potentials [17-19].

Si NW FETs are comprised of source, drain and gate electrodes. The conductivity changes in response to variations in the electric field or potential at the surface of the NW FET [9]. In a standard FET, a semiconductor, such as p-type silicon, is connected to high doped drain and

source with metal electrodes, through which under a given drain source voltage, a current is collected and injected, respectively. The conductance of the semiconductor between drain and source is controlled by a third gate electrode coupled through a thin dielectric layer [20]. Instead of the metal or polysilicon gate electrode, the gate voltage can be applied by an external electrode immersed in the aqueous solution as a solution gate. In the case of a p-Si or other p-type semiconductor, applying a negative gate voltage, which leads to negative charges at the interface between the gate electrode and dielectric, leads to an accumulation of carriers (positive holes) and a corresponding increase in conductance. However, applying a positive gate voltage to a p-type device, which leads to positive charges at the interface between the gate electrode and dielectric, will deplete carriers in the device and lead to a decrease in the conductance.

The NW FET sensing mechanism assumes a controlled modification in the local electric field of the channel, created by the binding of charged molecules on the NW surface. The high sensitivity of the Si NW nanosensors arises due to their small size and large surface-to-volume ratio. Conductance of Si NW changes remarkably upon the binding of even a small quantity of charged molecules [8].

The fabrication of Si NWs can be divided into two main categories: bottom-up and top-down [21]. The bottom-up approach relies on the assembly of pre-grown Si NWs [8, 22]. Vapor−liquid−solid (VLS) technology is the most commonly used method for bottom-up semiconductor NW production. The VLS mechanism relies on a vapor phase precursor of the nanowire material, which impinges on a liquid phase seed particle, from which unidirectional nanowire growth proceeds. The bottom-up approach has the advantage over top-down approaches that it avoids post-synthesis doping, such as ion implantation, which may destroy structures while introducing charge carriers. Consequently, bottom-up grown NWs may not require destructive techniques such as ion implanting to generate additional charge carriers. Additionally, it offers simplicity of NW production with low cost. On the other hand, bottom-up produced NW structures have a random distribution with different sizes. Such variability might imply a potential problem for complex chip integration of such NWs. Also, fabrication of ohmic contacts to a single nanowire is still not an easy task.

The top-down approach [23, 24] enables much more precise control of the geometry and electrical properties of Si NWs and more accurate alignment with other electrical components than the bottom-up methods. Top-down Si based devices fabrication is a well-established method, which has been optimized by the microelectronics industry for decades. In CMOS technology, these fabrication strategies use photolithography or related technology and dry etching to carve structures on a substrate. Therefore, novel applications of these techniques can be easily adopted by manufacturing of Si NWs with mass manufacturing ability. Indeed, Si NW FET based sensor integration with CMOS technology will reduce manufacturing costs. The intrinsic reliability of the well-established semiconductor CMOS technology also guarantees a reproducibility and reliability of proposed sensors.

Improving sensitivity is a major concern of modern development of the nanoscale sensor devices. Si NWs and nanometer-scale FETs have shown great sensitivity as chemical and biological FETs (Bio-FETs). However, according to Hooge's formula [25], with the downscaling of the nano device dimensions, the low frequency noise will increase inversely proportional to the characteristic size of the nano devices. This may result in degraded electrical characteristics. Therefore, it is necessary to diagnose the noise source of the sensor, and decrease the noise level to increase the signal-to-noise ratio (SNR).

In order to reach the detection limit, intense attempts have recently been made to understand the factors determining the SNR of Si NW FETs [26-28]. However, despite much work devoted to the discovering of noise in FETs, it is still not clear whether the carrier number fluctuations or mobility fluctuation approaches are adequate for the interpretation of noise in Si NW FETs [25, 29].

Therefore, a more detailed understanding of the noise properties (for example, low frequency noise source) is needed and hence developing a stable and reliable Si NWFET sensor with low-noise, cost-effective is of crucial importance. This PhD project is devoted to design, fabrication and characterization of Si NW FET sensor using a top-down approach which combines optimized thermal nanimprint (T-NIL) technology and tetramethylammonium hydroxide (TMAH) chemical etching. In order to study the dimension dependence of electrical and noise performance, Si NW FET devices with different length and width of nanowires were fabricated. The electrical and noise properties were studied using *I-V* characterization with a probe station and low frequency noise setup developed in house. Low frequency noise of the Si NW FET was measured to investigate the noise behavior and the minimum detectable charges of our devices. These results indicate that the number of detectable minimum charges on Si NW FET sensor of Si NW FET sensor increases proportionally with the square root of surface area of the NW. Random telegraph signals (RTSs) were registered in the Si NW FETs with submicron length. The characteristic parameters of the trap, such as depth, energy, capture and decapture time constants, can be extracted using the measured temperature dependence of low-frequency noise spectra and the time dependence of drain current fluctuations. Also, we find that the capture time of the RTSs can be used to monitor the changes of the surface potential on the NW surface with higher sensitivity compared with conventional technique based on the tracking of drain current changes.

1.2 Thesis Outline

In Chapter 1, firstly, I will give an introduction to the main subject of the PhD thesis. The advantages of NW devices and the motivation for choosing a top-down fabrication method are explained.

Chapter 2 describes important theoretical aspects of Si NW FET sensors and the origin of the main electric noise sources of FETs.

1.2 Thesis Outline

Chapter 3 provides an overview of the fabrication technology and low frequency noise measurement setup which have been used in this work.

Chapter 4 will present the fabrication technology of Si NW FETs. The imprint mold fabrication technology, the optimization of T-NIL and four kinds of design and processes are addressed in this chapter.

Chapter 5 gives the results of electrical and low frequency characterization of back gate Si NW FET devices with different channel length before and after gamma irradiation.

In Chapter 6, the modulation phenomena by single trap in Si NW FETs characterized using noise spectroscopy is described.

Chapter 7 describes the characterization results of Si NW FETs with 500 nm channel length. Coulomb blockade energy is extracted from these measurements.

Chapter 8 describes the noise properties and size dependence of sensitivity limits of Si NW biochemical sensors with micrometer channels.

Chapter 9 describes features of transport properties of submicrometer channel Si NW FETs. The dimension dependence of sensitivity in Si NW FET biosensors are given.

Chapter 10 describes the RTS noise as an analysis tool for high sensitive electrical biosensors application.

Chapter 11 concludes this thesis and gives an outlook for future improvements and applications of the Si NW FET biosensors.

2. Theoretical Background

Si NW FETs in their basic operation can be compared with the Ion-sensitive field-effect transistors (ISFET), which were proposed by Bergveld [30]. The operation of the ISFET is similar to the operation of the MOSFET device. Thus, in order to understand the operation of the Si NW FET, we will first discuss the fundamentals of the conventional MOSFET.

2.1 The MOSFET

Since the first experimental fabrication of the JFET (junction gate field-effect transistor) in 1947 shown in Figure 2.1 (a) [1], it revolutionized the field of electronics. Now the most commonly used transistor in today's integrated circuits is the metal oxide semiconductor field effect transistor (MOSFET) which was firstly invented in 1959 by DawonKahng and Martin M. (John) Atalla at Bell Labs [1, 2]. A typical n-type MOSFET is sketched in Figure 2.1 (b).

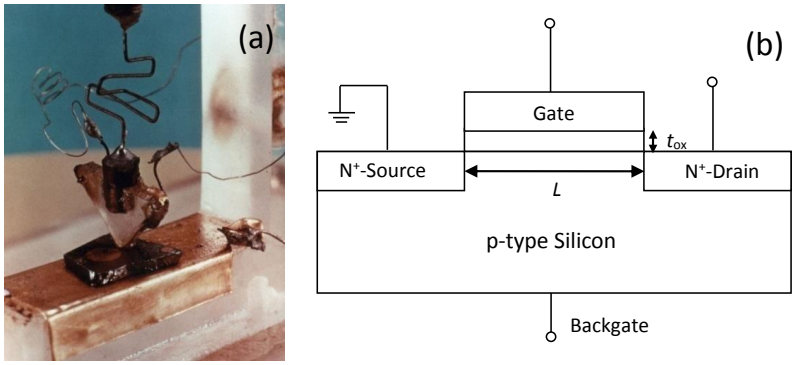


Figure 2.1 (a) The first transistor fabricated in 1947 at Bell Labs [1]. (b) Schematic of an n-type MOSFET device with the channel length *L* and gate oxide thickness t_{ox}.

The MOSFET is the key building block for modern integrated circuits in processors and dynamic memories. Although today the dimensions are much smaller than 30 years ago, nevertheless the operating modes and the basic principles are the same. Normally, a MOSFET is a four terminal device (Figure 2.1 (b)) with a source, drain, gate, and a substrate or body contact [20]. The n-MOSFET is implemented on a p-type bulk silicon crystal with two highly doped n^+ regions, which act as source and drain contacts. The area between source and drain regions is called the channel and it is covered with a dielectric layer and then a metal or polisilicon contact on top, called the gate electrode. The surface potential of the channel determines the conductivity between the source and drain terminals. If we apply voltage between the source and drain regions, it results in the appearance of a bias electric field in the channel and thus a drift current flows through the channel of the device. By applying a bias to the gate electrode, the surface potential of the channel can be changed, and therefore the current between source and drain is modulated.

2.1.1 Electrical Characteristics

As it was mentioned before, for simplicity, the MOSFET is described as a three terminal device with source, gate and drain. The current goes through the drain and source terminals and is controlled by the gate terminal.

The threshold voltage can be defined as [20]

$$V_{Th} = \frac{\phi_M - \phi_{Si}}{q} - \frac{Q_{ox} + Q_{it} + Q_{dep}}{C_{ox}} + 2\phi_f \tag{2.1}$$

where ϕ_M and ϕ_{Si} are the work functions of the gate electrode and the silicon, respectively. Q_{ox}, the oxide charge, Q_{it}, the Si/SiO_2 interface charge, and Q_{dep}, the depletion layer charge in the silicon, C_{ox} is the capacitance per unit area, and ϕ_f accounts for the difference in Fermi level between doped and intrinsic silicon.

If the gate voltage is smaller than the threshold voltage ($V_{GS} < V_{Th}$), the source to channel barrier is large and the number of charge carriers in the channel is small. In this case, the diffusion of the charge carriers dominates and the drain current I_{DS} varies exponentially with ($V_{GS} - V_{Th}$) as given by [20]

$$I_{DS} = \frac{W}{L}\mu_{eff}\left(C_{it} + C_{dep}\right)\left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{GS}-V_{Th})}{mkT}} \tag{2.2}$$

where $m = 1 + \frac{C_{it}+C_{dep}}{C_{ox}}$, μ_{eff} is effective mobility, and W and L is the width and length of the channel, respectively, *k* is the Boltzmann constant, *q* is the elementary charge and *T* is the absolute temperature.

The subthreshold slope, is defined as the gate-source voltage needed to increase the drain current by one order of magnitude in subthreshold region [20]

$$S = \frac{dV_{GS}}{d(logI_{DS})} = ln\,10\frac{dV_{GS}}{d(lnI_{DS})} = 2.3m\frac{k_bT}{q}(mV/decade) \tag{2.3}$$

Obviously, the smallest value of *S* will be achieved if *m* equals unity. Accordingly, the theoretical lower limit of the subthreshold slope is 60 mV/decade at room temperature.

When $V_{GS} > V_{Th}$, an inversion layer of hole carriers is formed under the oxide layer of the channel, thus, creating a conducting channel between source and drain. The density of holes (Q_p) in the inversion layer per unit area parallel to the surface over the entire channel length *L* is given by [20]

$$Q_p = WC_{ox}(V_{GS} - V_{Th}) \tag{2.4}$$

In this equation, W is the width of a transistor, C_{ox} is the gate oxide capacitance per unit area, and V_{GS} and V_{Th} are the gate source voltage and threshold voltage, respectively.

An applied drain-source voltage causes Q_p to vary along the length of the channel because the voltage drop across the gate oxide is now a function of the channel length. Assuming that the voltage drop at position x along the channel length is $V(x)$, the hole density at position x is given by [31]:

$$Q_p(x) = WC_{ox}[V_{GS} - V(x) - V_{Th}] \tag{2.5}$$

while the current at position x is equal to

$$I_{DS} = WC_{ox}[V_{GS} - V(x) - V_{Th}]\mu_{eff}\frac{dV(x)}{dx} \tag{2.6}$$

Since I_{DS} remain constant along the channel, in long channel simple model, we assume the mobility, μ_{eff}, to be constant.

Integrating both sides of Equation (2.6) over the length of the channel. The resulting relation between the drain current as a function of drain-source voltage, V_{DS}, and gate-source voltage, V_{GS}, is given by

$$I_{DS} = C_{ox}\mu_{eff}\frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{2.7}$$

As we can see, I_{DS} is not a linear function of drain voltage. However, for a small drain voltage, Equation (2.7) reduces to:

$$I_{DS} = C_{ox}\mu_{eff}\frac{W}{L}(V_{GS} - V_{Th})V_{DS} \tag{2.8}$$

In operation, $C_{ox}\mu_{eff}W/L$ is determined by the material and design of the device. V_{Th} remains constant for a given device and represents the value which surface potential should overcome to open the transistor. Therefore, if V_{DS} and V_{Th} are held constant and only V_{GS} is varied, one arrives at a function for drain current dependent only on V_{GS}. The Equation (2.8) exhibits a linear relation between I_{DS} and V_{DS} for a given V_{GS} and the transistor behaves simply like a resistor.

If the drain voltage increases, the drain current I_{DS} reaches a saturation and becomes constant when $|V_{DS}| > |V_{GS} - V_{Th}|$. At the point where $V_{DS} = V_{GS} - V_{Th}$, the channel experiences a pinch-off state. Thus, a further increase in V_{DS} simply shifts the pinch-off point toward the drain terminal. In the saturation mode, the relation between the drain current and the voltage is given by

$$I_{DS} = C_{ox}\mu_{eff}\frac{W}{L}(V_{GS} - V_{Th})^2 \tag{2.9}$$

This equation applies for a long channel transistor, while the equation must be modified considering the channel modulation effect for a short channel transistor.

The transconductance, g_m, of a MOSFET is a measure of the gate's control over channel current modulation. It is given by the first derivative of I_{DS} with respect to V_{GS} and can be determined from the transfer characteristic of the device [20]:

$$g_m = \frac{\partial I_{DS}(V_{GS})}{\partial V_{GS}}\Big|_{V_{DS}=const} \tag{2.10}$$

In general, g_m is inversely proportional to the gate length, L, and directly proportional to the gate with, W, in the linear region of the I_{DS} vs V_{GS} curve.

2.2 The ISFET

2.2.1 Comparison to MOSFET

The schematical representation of a MOSFET and an ISFET is illustrated in Figure 2.2, instead of the metal gate, in ISFET, the gate voltage is applied via a reference electrode via electrolyte. The threshold voltage of the transistor is then defined by the reference electrode potential E_{ref}, the surface potential, ψ_s, and surface dipole potential of the solution, χ^{sol}. Value of ψ_s is determined from the outcome of a chemical reaction, usually governed by the dissociation of surface-oxide groups, χ^{sol} is the surface dipole potential of the solvent having a constant value. Therefore, the threshold voltage for an ISFET becomes [32]

$$V_{Th} = E_{ref} - \psi_s + \chi^{sol} - \frac{\phi_{Si}}{q} - \frac{Q_{ox} + Q_{it} + Q_{dep}}{C_{ox}} + 2\phi_f \tag{2.11}$$

which is similar to Equation (2.1) except the terms $E_{ref} - \psi_s + \chi^{sol}$ which appear due to presence of the electrolyte on the top of the ISFET, all terms in this equation are constant besides ψ_s, which makes the ISFET device sensitive to the analyte in electrolyte. Q_{ox}, Q_{it} and Q_{dep} are the oxide charge, interface charge and depletion layer charge in the silicon, C_{ox} is the capacitance per unit area, and ϕ_f accounts for the difference in Fermi level between doped and intrinsic silicon.

The surface potential of the gate depends on the oxide-liquid interface, where the surface charge is determined by the dissociation of the oxide surface groups at different pH values of the solution or by the adsorption of charged molecules from the solution on the surface. Then, assuming fixed drain and gate voltages and reference electrode potential, the drain current is only dependent on ψ_s. Therefore, the ISFET is sensitive to the pH value of the electrolyte or the binding of charged biomolecules presented in the solution.

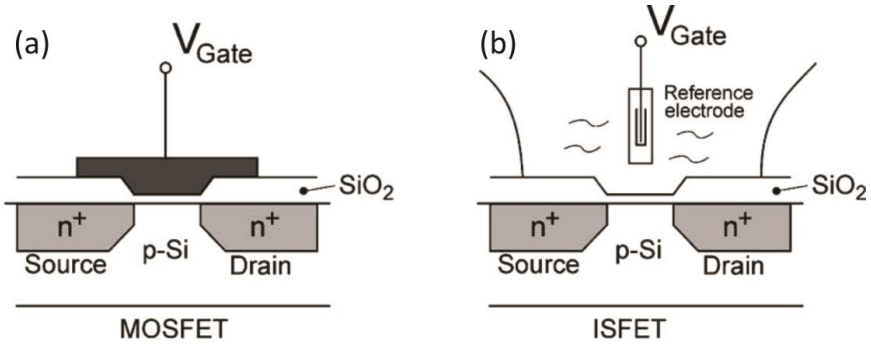


Figure 2.2 Schematic representation of MOSFET (a), ISFET (b) [32].

The dependence of the drain source current (I_{DS}) on the drain-source voltage (V_{DS}) at constant gate-source voltages (V_{GS}) is called "output characteristics". Figure 2.3 shows the typical output characteristics of a p-channel ISFET measured in an electrolyte solution of 0.01 mM phosphate buffered saline (PBS) as gate voltage is varied from -1 V to -3 V in a step of 0.5 V. At low V_{DS}, the current shows linear dependence on V_{DS}, while at high V_{DS} the current is saturated due to channel pitch-off, described above (see Equation (2.9)) and only depends on V_{GS}.

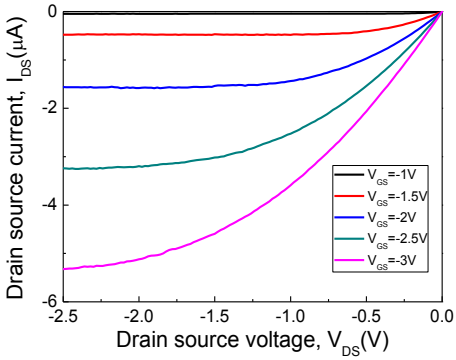


Figure 2.3 Output characteristics of a p-channel ISFET device show the dependence of current on V_{DS} at constant V_{GS} values. At low V_{DS} the transistor behaves like a resistor while at high V_{DS} the current I_{DS} saturates.

The dependence called "transfer characteristic" displays the I_{DS} versus V_{GS} at constant V_{DS}. Figure 2.4 shows the transfer characteristics of the p-channel ISFET in linear and in logarithmic scales. On a linear scale, we can see that essentially no current flows until the gate voltage reaches the threshold voltage. However, if we have a closer look at the subthreshold region $V_{GS} < V_{Th}$ on the logarithmic scale, we will see that the drain current increases exponentially with increasing voltage.

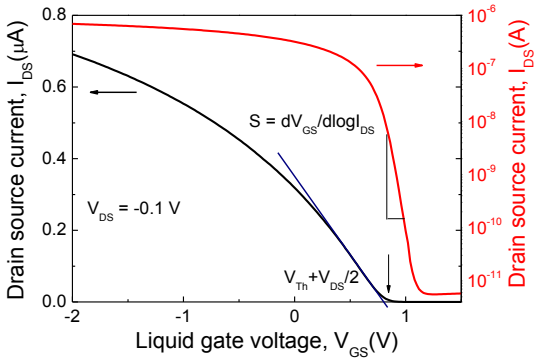


Figure 2.4 Transfer characteristics of a p-channel ISFET showing I_{DS} on a linear scale(black) and a logarithmic scale (red) as a function of liquid gate voltage, V_{GS}. Subthreshold slope S and the threshold voltage V_{Th}.

2.2.2 Modeling of the Oxide/Electrolyte Interface

The ISFET is an open gate structure exposed to the electrolyte solution. Thus, mobile ions and molecules in the electrolyte can approach or undergo a reaction with the surface of the FET. Modeling of the Oxide/Electrolyte interface is based on ideas introduced in the literatures of Ref. [33, 34].

In the case of differing pH value of the electrolyte, the hydroxyl groups on the oxide surface of the FET channel are charged depending on the pH-value of the solution, this will either increase or decrease the channel conductance. It is well-known that the outer surface of an oxide contains a layer of amphoteric hydroxyl groups (-MOH), where M refers to a surface site occupied by a metal ion [35]. In the case of SiO_2 or Al_2O_3, -MOH refers to the Si-OH group and Al-OH group, respectively. In aqueous solution, these groups interact with protons (H^+) in the solution. This model known as the site-binding model was first introduced by Yates et al. [36] and was later refined by Healy et al. [37]. Depending on the isoelectric point (IEP) of the surface, the point where the surface is neutral (surface potential equals 0), and the pH of the solution, these hydroxyl groups can be either neutral, protonized (positively charged) or deprotonized (negatively charged) due to dissociation of the surface hydroxyl group. By donating or accepting a proton to or from the solution the (-MOH) groups are able to undergo reactions, which can be described as:

$$\mathrm{MOH} \rightleftarrows \mathrm{MO^-} + \mathrm{H^+}, \tag{2.12}$$

$$\mathrm{MOH_2^+} \rightleftarrows \mathrm{MOH} + \mathrm{H^+} \tag{2.13}$$

The equilibrium conditions are described by

$$K_a = \frac{[AO^-] \cdot [H_S^+]}{[AOH]} \tag{2.14}$$

$$K_b = \frac{[AOH] \cdot [H_S^+]}{[AOH_2^+]} \tag{2.15}$$

where each of values in square brackets $[AO^-]$, $[AOH]$ and $[AOH_2^+]$ denote the concentration of the different protonation states on the surface, and $[H_S^+]$ is the concentration of hydrogen ions at surface. K_a and K_b are the intrinsic constants for specific oxide surfaces, which for silicon oxide are reported around 2 and 6.8, respectively [33]. This yields a point of zero surface charge for the pH, $pH_{pzc} = \frac{1}{2}(K_a + K_b) = 2.4$ for SiO_2. Consequently, at physiological pH values (pH ≈ 7), the net surface charge of silicon oxide is negative. $[H_S^+]$ is related to the concentration of hydrogen ion in the bulk solution through the Boltzmann equation:

$$[H_S^+] = [H_B^+] e^{-q\psi_{SB}/kT} \tag{2.16}$$

where $[H_S^+]$ and $[H_B^+]$ is the concentration of hydrogen ions (H^+) at the surface and in the bulk solution, respectively, q is the elementary charge, ψ_{SB} is the electrostatic potential difference between the silicon oxide surface and the bulk of electrolyte solution, k is the Boltzmann constant and T is the absolute temperature. From the Boltzmann equation, one can describe the pH dependence of ψ_{SB} using the Nernst equation, which describes the relation at equilibrium between ψ_{SB} and the differences in the pH-value between the bulk and surface:

$$\psi_{SB} = 2.3\frac{kT}{q}(pH_S - pH_B) \tag{2.17}$$

The surface charge density σ_0 is the product of the elementary charge and the difference between the number of negatively and positively charged groups per unit area. The surface charge density is:

$$\sigma_0 = q([AOH_2^+] - [AO^-]) \tag{2.18}$$

Defining the number of sites per unit area as N_S, since the oxide surface can be any polarity, the number of surface sites is the sum of the concentration of each possible state:

$$N_S = [AO^-] + [AOH_2^+] + [AOH] \tag{2.19}$$

From Equations (2.14) - (2.19), The surface charge density is given by:

$$\sigma_0 = qN_s\left(\frac{[H_S^+]^2 - K_aK_b}{K_aK_b + K_b[H_S^+] + [H_S^+]^2}\right) \tag{2.20}$$

Changing the surface pH by a small amount, (∂pH_S), then results in a change of the surface charge density:

$$\frac{\partial \sigma_0}{\partial pH_S} = -q\beta_{int} \tag{2.21}$$

where β_{int} is the intrinsic buffer capacity of the oxide surface. This capacity is a local effect and is only capable of buffering small changes in the pH at the surface. On the liquid side of the surface (and for reasons of charge neutrality) the surface charge forms in the electrolyte next to the oxide to counter the charge that is accumulated on the device surface. The charge in this double-layer, σ_{dl}, is equal to σ_0 but with the opposite sign, $\sigma_{dl} = -\sigma_0 = -C_{DL}\psi_{BS}$. Here C_{DL} defines the integral double-layer capacitance and can be calculated using the Gouy-Chapman-Stern model [38-40]. The differential capacitance, which represents the ability to store charge in response to a small changes in the electrostatic potential, can then be defined as:

$$\frac{\partial \sigma_0}{\partial \psi_{SB}} = \frac{\partial \sigma_{dl}}{\partial \psi_{SB}} = C_{DL} \tag{2.22}$$

The combination of Equation (2.21) and Equation (2.22) gives the change of the surface potential due to a small change in surface pH:

$$\frac{\partial \psi_{SB}}{\partial pH_S} = \frac{\partial \psi_{SB}}{\partial \sigma_0}\frac{\partial \sigma_0}{\partial pH_S} = \frac{-q\beta_{int}}{C_{DL}} \tag{2.23}$$

From the Nernst equation (2.17), we can get:

$$\frac{\partial pH_S}{\partial pH_B} = \frac{\partial pH_S}{\partial\left(pH_S - \frac{\partial \psi_{SB}}{2.3\frac{kT}{q}}\right)} = \frac{1}{1 - \frac{1}{2.3\frac{kT}{q}}\cdot\frac{\partial \psi_{SB}}{\partial pH_S}} \tag{2.24}$$

By combining Equation (2.24) and Equation (2.23) the general equation for an ISFET's sensitivity to pH can be obtained:

$$\frac{\partial \psi_{SB}}{\partial pH_B} = \frac{\partial \psi_{SB}}{\partial pH_S}\frac{\partial pH_S}{\partial pH_B} = -2.3\frac{kT}{q}\alpha \tag{2.25}$$

with

$$\alpha = \frac{1}{\frac{2.3kTC_{DL}}{q^2\beta_{int}} + 1} \tag{2.26}$$

A change in the bulk solution's pH affects the potential at the surface, which can be measured by the ISFET. α is a dimensionless sensitivity parameter varying between 0 and 1. It depends on the intrinsic buffer capacity β_{int} and the double layer capacitance C_{DL}. In the ideal case, $\alpha = 1$, we will achieve the maximum sensitivity of 59.5 mV/pH at 300 K, also known as the "Nernst limit". We note here that β_{int} depends on the gate oxide used as the interface layer.

2.3 Si NW FET Biosensors

When shrinking the channel of ISFET to nano size dimension, Si NW FET biosensor was obtained. Since the first report on the biosensing ability of Si NW FETs in 2001 [41], extensive research efforts have been initiated to develop NW-based biosensors [8, 11-15, 18, 23, 42-47]. The extremely large surface-to-volume ratio of one-dimensional nanostructures makes it possible to develop biosensors with exquisite sensitivity [8]. Any small disturbance of, or adsorption to, the surface may result in a large change in electrical conductance. Already, biosensors fabricated with semiconducting NWs have been used as sensors that can detect single virus [16], nucleic acids [15] and proteins in solution [13, 14] as well as biochemical signaling events from cells or neuronal action potentials [17-19]. The mechanism of sensing is based on the changes of sensor conductance in response to the specific binding of (bio) chemical molecules to the sensor inducing a potential change on the gate oxide surface and then modulating the number of charge carriers or conductance in the NW channel.

There are two strategies to fabricate NW FETs, top-down and bottom-up approaches. In top-down approach, the NWs and the electronic circuitry including drain and source, are all fabricated from a bulk silicon wafer using advanced microelectronics technologies (i.e. lithography, etching, and deposition). These technologies are mature and reliable. In bottom-up approach, NW building blocks are synthesized before and randomly distributed onto the chip surface, which provides much greater flexibility in NW material electrical properties, so it has a lower reproducibility and reliability compared with top-down approach.

In top-down approach, Stern *et al.* reported a complementary metal oxide semiconductor (CMOS) compatible technology to fabricate Si NW FET biosensor which can detect antibodies with 100 fM concentration [23]. An anisotropic wet etch was used instead of reactive ion etching (RIE), to avoid the device degradation that RIE may induce [48]. The resulting Si NWs had trapezoidal cross-sections with nm-scale width and height.

Lieber's group has pioneered bottom-up approach to fabricate Si NW FET biosensors [13, 15, 49]. In that work, boron-doped p-type Si NW devices grown by the vapor–liquid–solid (VLS) method were covalently modified with 3-amino-propyltriethoxysilane (APTES). APTES can undergo protonation and deprotonation according to the pH value in the medium. Since then, numerous FET based biosensors that use semiconductor NW FETs or carbon nanotube field effect transistors (CNTFETs) have been demonstrated due to their ultrasensitive, label-free, real-time electrical detection of biomolecules.

2.4 Noise Characterization

2.4.1 Fundamentals of Noise Mechanisms

In electronics, noise is inherent to any devices and appears as a random fluctuation in all electrical signals. It is impossible to be totally eliminated, but it can be reduced by the proper design of devices and circuits. The intensity of the fluctuations depends on device type, the manufacturing processing, and the operating conditions.

Unlike deterministic signals, random signals cannot be predicted. Figure 2.5 illustrates how an electronic signal fluctuates randomly due to noise component. The current through a device can be described as [50]:

$$I(t) = \bar{I} + i_n(t) \tag{2.27}$$

where $\bar{I}$ is the average current and $i_n(t)$ is a randomly fluctuating current that provides the noise based component in the form of a randomly fluctuating current. The average of $i_n(t)$ measured over a long time is always equal to zero. The value of $i_n(t)$ at any point in time cannot be predicted due to its random origin property. The study of noise has its roots in the mathematical methods from probability theory, a common approach to handling noise analysis is to convert the signal from the time domain to the frequency domain by Fourier transformation. It allows the definition of appropriate average value of current noise.

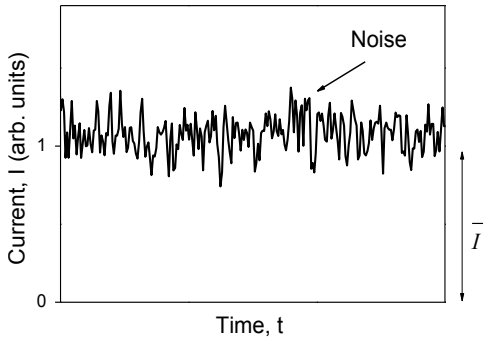


Figure 2.5 A typical noise waveform is illustrated [50].

2.4.1.1 Power Spectral Density

The noise signal is usually a time independent event that manifests in the time dependent recorded voltage or current signal, as shown in Figure 2.5. The Fourier transforms of the noise signal give the power per unit frequency, known as power spectral density (PSD) of the signal, which describes how the power of a time series signal is distributed over the different frequencies. For voltage signals, it is customary to use units of V^2/Hz for the PSD. In our case, the PSD is measured with a spectrum analyzer from a time series signal.

Noise with a constant PSD of $S(f)$ for all frequencies is referred to as "white noise". It is usually observed that the PSD of noise is dependent on frequency at low frequencies up to the corner frequency and becomes white thereafter. A schematic diagram of the PSDs for low frequency noise in excess of the underlying white noise is shown in Figure 2.6. The excess low-frequency noise may consist of $1/f$ noise (or $1/f$ like noise) and generation-recombination (G-R) noise [50].

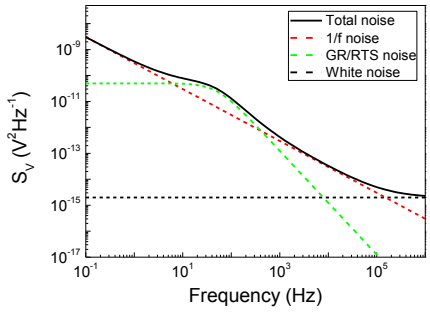


Figure 2.6 The PSD (S_V) of excess low-frequency noise and white noise as a function of frequency. The excess noise above the white noise floor may consist of either or both $1/f$ noise and G-R/RTS noise [50].

While both white noise and excess low-frequency noise must be considered in electronic circuit development and their relative importance varies according to different types of circuit and its application. The physical mechanisms behind the white noise sources are well known and the white noise level can usually be accurately predicted in electronic circuits. However, the origin of the excess low-frequency noise is a hot topic of investigation with many challenges remaining [50]. For this reason, this thesis mainly deals with excess low-frequency noise.

2.4.1.2 Noise Quantification

The PSD discussed above provides information about how the noise power is distributed in the frequency domain. The PSD of the current noise and voltage noise has units of A^2/Hz and V^2/Hz, respectively. We term the mean square of noise voltage or noise current the noise power, and this value can be considered as the average power delivered to a ohmic resistor within the bandwidth of the system, Δf, from a fluctuating current or voltage. The RMS (root

mean square) voltage noise is the square root of the voltage noise power over the frequency [50]:

$$V_{n,rms} = \sqrt{\overline{V_n^2}} = \sqrt{\int_{f_1}^{f_2} S_V df} \approx \sqrt{\frac{1}{T}\int_0^T V_n^2(t)dt}, \tag{2.28}$$

where V_n is the voltage noise, and S_V is the PSD of the voltage noise and $\Delta f = f_2 - f_1$. The last expression suggests how $V_{n,rms}$ can be measured in terms of a value recorded over time. However, it is important that the averaging time, T, is long enough.

2.4.2 Noise Sources

Several basic physical phenomena can cause random fluctuations in the current (or voltage) of a device, generating random noise. Since the charge transported through a conductor in a given unit of time defines the current, the average current through a piece of conductive material with length L can be written as [50]:

$$\overline{I} = \frac{q\overline{N}\overline{v}}{L} \tag{2.29}$$

where q is the elementary charge, N is the number of free carriers in the slab and v is the drift velocity of the carriers. Here, and hereafter, a bar over a variable always denotes the average of that variable is taken. Both N and v can fluctuate, therefore as discussed by Von Haartmann and Oestling [50]:

$$I(t) = \sum_{i=1}^{N(t)} q\frac{v_i(t)}{L} \tag{2.30}$$

where v_i is the drift velocity of an individual carrier and:

$$N(t) = \overline{N} + \Delta N(t) \tag{2.31}$$

$$v_i(t) = \overline{v_i} + \Delta v_i(t) \tag{2.32}$$

For a homogeneous sample in the presence of a uniform electric field, the average drift velocity is the same for each carrier. The current fluctuation can be written as:

$$\Delta I(t) = \frac{q}{L}\overline{v}\Delta N(t) + \frac{q}{L}\sum_{i=1}^{\overline{N}} \Delta v_i(t) \tag{2.33}$$

The first term accounts for variation in the number of carriers and the second term describes the fluctuating carrier velocity. The drift velocity is proportional to the applied electric field $v = \mu E$ or more generally $v = \mu_i E$. Here, the subscript *"i"* has the meaning "individual" and the proportionality constant, μ, is the carrier mobility, while μ_i is the individual carrier mobility. So these are two primary sources of noise current fluctuations that originate from carrier number fluctuation and carrier mobility fluctuation.

2.4.2.1 Thermal Noise

Thermal noise (Nyquist, Johnson noise) is generated by the random thermal motion of charge carriers in a material, which happens regardless of any applied voltage as the electron drift velocity is much less than the electron thermal velocity [51].

An electron's velocity is randomized each time it undergoes scattering. Due to these randomized changes in speed and direction, there could suddenly be more electrons moving in a certain direction than electrons moving in the other directions, which would generate a small net current. This current fluctuates in intensity and direction in such a way that taken over a long time, the average current is always zero. Considering a piece of material with resistance R at temperature T, the PSD of the thermal noise current can be presented as:

$$S_I = \frac{4kT}{R} (or\ S_V = 4kTR) \tag{2.34}$$

The power spectral density of thermal noise is thus clearly proportional to the absolute temperature, and both approach zero together. However, in the frequency domain, the white noise PSD is roughly constant over the whole spectrum [51].

2.4.2.2 Shot Noise

The shot noise was first discovered in vacuum tubes by W. Schottky in 1918 [52]. The movement of discrete charge carriers forces the current across a potential barrier, such as a p-n junction, to be discontinuous in nature. A shot noise current is generated when the electrons cross the barrier independently and at random. The current fluctuates with a PSD:

$$S_I = 2qI \tag{2.35}$$

where I is the DC current across the barrier [52].

2.4.2.3 Generation-recombination Noise

G-R noise in semiconductors stems from traps due to generation-recombination processes, thereby causing fluctuations in the number of carriers available in the channel [50]. The trapped charge can also induce fluctuations in other properties, such as the carrier mobility, diffusion coefficient, electric field, barrier height, space charge region width, etc. Defects or impurities in the semiconductor bulk, or surface of the material generate electronic states within the forbidden band gap and are referred to as traps.

The PSD of the fluctuations in the number of carriers can be described as [50]:

$$S_N(f) = 4\overline{\Delta N^2}\frac{\tau}{1+(2\pi f)^2\tau^2} \tag{2.36}$$

Here, τ is the time constant of the transitions. The shape of the spectrum given by Equation (2.36) is called a Lorentzian and is illustrated in Figure 2.8 (black curve) in the next section. G-R noise is only significant when the Fermi energy level is close, within a few kT, to the trap energy level. In that case, the capture time τ_c and the emission time τ_e are almost equal. If the Fermi-level is not near the trap level, the trap will be filled or empty most of the time and few transitions will occur that produce noise. The variance can be expressed as [25]:

$$\frac{1}{\overline{\Delta N^2}} = \frac{1}{N} + \frac{1}{N_{T,full}} + \frac{1}{N_{T,empty}} \tag{2.37}$$

where N is the number of the carriers in the channel , $N_{T,full}$ and $N_{T,empty}$ are the average number of full and empty traps, respectively. At the Fermi level and assuming $N \gg N_T$ where $N_T = N_{T,full} + N_{T,empty}$ [50]:

$$\overline{\Delta N^2} = \frac{N_T}{4} \tag{2.38}$$

Using Equations (2.36), (2.37) and (2.38), one can arrive at:

$$\frac{S_N}{N^2} = \frac{N_T}{N^2}\frac{\tau}{1+(2\pi f)^2\tau^2} \tag{2.39}$$

Since N is proportional to the current:

$$\frac{S_I(f)}{I^2} = \frac{S_N(f)}{N^2} = \frac{N_T}{N^2}\frac{\tau}{1+(2\pi f)^2\tau^2} \tag{2.40}$$

As seen from Equation (2.40), the PSD is proportional to the number of traps and inversely proportional to the number of carriers squared. In general, the time constant and the relative strength of the traps differ (depending on the trap energy level and spatial position).

2.4.2.4 Random Telegraph Signal Noise

The Random Telegraph Signal (RTS) phenomenon is commonly related to the activity of a single [53] or a few traps [54] undergoing trapping and detrapping processes in a system with

few free carriers [55]. The charge state may be changed from the neutral to the repulsive charge (neutral trap) or from an attractive to a neutral charge (attractive trap) [56]. As such, it is a special case of G-R noise. If only one trap is involved, the current can switch between two states due to the random trapping and detrapping of carriers. This process is displayed as discrete switching events between two discrete states in the time domain, see Figure 2.7.

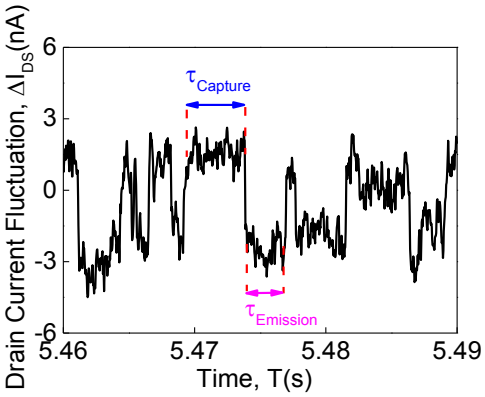


Figure 2.7 Time dependence of RTS noise, typically observed for a MOSFET. The drain current switches between two discrete levels when a channel electron is captured and decaptured by a trap in the gate oxide.

The corresponding current noise spectrum to Figure 2.7 is derived as:

$$S_I(f) = \frac{4\Delta I^2 \tau^2}{(\tau_c + \tau_e)[1 + (2\pi f \tau)^2]} \tag{2.41}$$

where ΔI is the switching current amplitude [53]. The characteristic time constant τ is determined by the average capture time τ_c and the average emission time τ_e through:

$$\frac{1}{\tau} = \frac{1}{\tau_c} + \frac{1}{\tau_e} \tag{2.42}$$

Figure 2.8 (black curve) shows the Lorentzian PSD of the RTS noise waveform in Figure 2.7. It is obvious that the PSD of RTS noise is of the Lorentzian type. G-R noise can be viewed as a sum of RTS noise processes from various traps whose time constants are the same, and is only displayed as RTS noise in the time domain if the number of traps involved is small.

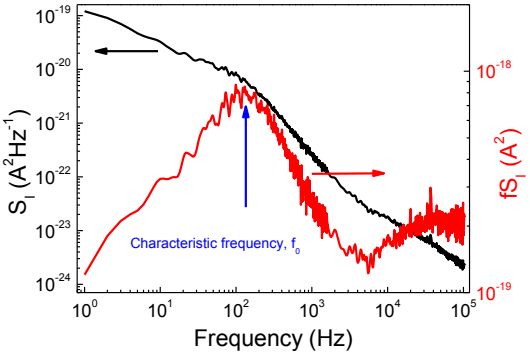


Figure 2.8 Lorentzian shaped PSD and multiplied by frequency, plotted for the RTS noise waveform taken from the current shown in Figure 2.7.

The characteristic Frequency, f_0, depicted in Figure 2.8 (red curve), can be most easily derived by plotting $f \times S_I$ as a function of f, which yields a maximum at $f = f_0$. Then the characteristic time constant τ is given by:

$$f_0 = \frac{1}{2\pi\tau} \tag{2.43}$$

2.4.2.5 1/f Noise

$1/f$ noise, also commonly called flicker noise, are the fluctuations that occur with a power spectral density proportional to $f = 1/f^{\gamma}$ with γ close to 1 at low frequency. The PSD of $1/f$ noise takes the general form [50]:

$$S_I = \frac{KI^{\beta}}{f^{\gamma}} \tag{2.44}$$

where K is a constant value and β is a current exponent. $1/f$ fluctuations have been described in the conductance of various conductors and semiconductors at low-frequencies.

The origin of the $1/f$ noise observed in MOSFETs remains a topic of debate despite a half century of investigation on the phenomena. The discussion returns to the two conflicting possible physical mechanisms behind any fluctuations in the current: fluctuations in the mobility and fluctuations in the number of carriers [57].

2.4.2.5.1 Number Fluctuation

The physical mechanism of the number fluctuation $1/f$ noise is due to G-R noise in the electron transitions between the conduction band of the channel material and the traps in the oxide layer of the MOSFET [50, 57, 58]. The surface potential oscillates as the oxide traps

dynamically exchange carriers with the channel. This exchange causes fluctuations in the inversion charge density. If a drain current is flowing in the device, these fluctuations are translated to the current and can be observed in measurements. The fluctuating oxide charge density, Q_{ox}, is equivalent to a variation in the flat-band voltage, V_{fb} [50],

$$\delta V_{fb} = -\frac{\delta Q_{ox}}{C_{ox}} \tag{2.45}$$

Employing the equation for the fluctuation in the drain current, $I_{DS} = f(V_{fb}, \mu_{eff})$, then we can get [50, 59]:

$$\delta I_{DS} = \frac{\partial I_{DS}}{\partial V_{fb}} \delta V_{fb} + \frac{\partial I_{DS}}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \tag{2.46}$$

Since $\partial I_{DS}/\partial V_{fb} = -\partial I_{DS}/\partial V_{GS} = -g_m$($-g_m$ for p MOS) and $I_{DS} \propto \mu_{eff}$ [50, 59]:

$$\delta I_{DS} = -g_m \delta V_{fb} + \frac{I_D}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \tag{2.47}$$

One can further define a parameter, α that reflects how variation in the oxide charge is coupled to the mobility [50, 59]:

$$\alpha = \frac{1}{\mu_{eff}^2} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \tag{2.48}$$

which is valid for n-type MOSs. Conversely, a minus sign has to be used for p-type MOSs.

Inserted in Equation (2.47) (for n-type MOSFETs) this gives [50, 59]:

$$\delta I_{DS} = -g_m \delta V_{fb} - I_D \mu_{eff} \alpha C_{ox} \delta V_{fb} \tag{2.49}$$

The power spectral density is then given by [50, 59]:

$$S_{I_{DS}} = S_{V_{fb}} \left(1 + \frac{I_{DS} \mu_{eff} \alpha C_{ox}}{g_m}\right)^2 g_m^2 \tag{2.50}$$

The first term in Equation (2.50) is due to the fluctuating number of inversion carriers and the second term is due to mobility fluctuations correlated with the number fluctuations. Note that

α can be negative or positive depending on if the mobility increases or decreases upon trapping a charge according to Equation (2.48).

The normalized spectral density of the drain current can then be derived as [50, 59]:

$$\frac{S_{I_{DS}}}{I_{DS}^2} = S_{V_{fb}}\left(1 + \frac{I_{DS}\mu_{eff}\alpha C_{ox}}{g_m}\right)^2 \frac{g_m^2}{I_{DS}^2} \tag{2.51}$$

The equivalent input gate voltage spectral density is given by [50, 59]:

$$S_{U_g} = S_{V_{fb}}\left(1 + \frac{I_{DS}\mu_{eff}\alpha C_{ox}}{g_m}\right)^2 \tag{2.52}$$

It is clear from Equation (2.52) that if the mobility is almost independent of interface charge $(\alpha \approx 0)$, as $S_{V_{fb}}$ is weakly bias dependent, then $S_{U_g} = S_{V_{fb}}$ and $S_{I_{DS}}/I_{DS}^2$ essentially varies as g_m^2/I_{DS}^2. In contrast, for high enough values of α, the second term cannot be neglected so that the input gate voltage spectral density could be very different from $S_{V_{fb}}$and S_{I_DS}/I_{DS}^2 may not be well correlated to g_m/I_{DS}^2.

2.4.2.5.2 Mobility Fluctuation

In contrast to the number fluctuation model, the Hooge mobility fluctuation model states that the fluctuations of the drain current arise from the fluctuations of the carrier mobility [60]. This results in a flicker noise, whose intensity is inversely proportional to the total number of carriers in the system [58, 60]. Therefore, the drain current noise generated by fluctuations in the channel carrier mobility is given according to Hooge's empirical formula [50, 59]:

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{q\alpha_H}{fN} \tag{2.53}$$

where α_H is the Hooge parameter, which can often be considered as a constant, and N is the number of the carriers in the channel. If N is replaced by WLQ_i/q, in the linear region $Q_i = C_{ox}(V_{GS} - V_{Th})$, the normalized drain current noise can be calculated as [50, 59]:

$$\frac{S_{I_{DS}}}{I_{DS}^2} = \frac{\alpha_H}{fWLC_{ox}(V_{GS} - V_{Th})} \tag{2.54}$$

Equation (2.54) only holds true for uniform carrier density. It is obvious that normalized drain current noise depends inversely on the gate voltage overdrive in the linear region.

The corresponding input gate voltage spectral density is thus given by [50, 59]:

$$S_{U_g} = \frac{S_{I_{DS}}}{I_{DS}^2}\frac{I_{DS}^2}{g_m^2} \tag{2.55}$$

Then [50, 59]:

$$S_{U_g} = \frac{q\alpha_H}{fWLQ_i}\frac{I_{DS}^2}{g_m^2} \tag{2.56}$$

In the case of strong inversion, the inversion charge reduces to $Q_i = C_{ox}(V_{GS} - V_{Th})$ and for a small drain voltage, the drain current transconductance ratio reduces to $I_{DS}/g_m = V_{GS} - V_{Th}$, so that the input gate voltage spectral density can be expressed as [50, 59]:

$$S_{U_g} = \frac{q\alpha_H}{fWLC_{ox}}(V_{GS} - V_{Th}) \tag{2.57}$$

Therefore, in the case of Hooge mobility fluctuations, the input gate voltage spectral density has a linear relation to the gate voltage. Moreover, the inverse of the normalized drain current spectral density may simply be proportional to the overdrive gate voltage $(V_{GS} - V_{Th})$ [50].

3. Materials and Methods

Si NW FET devices were fabricated at the cleanroom of the Helmholtz Nanoelectronic Facility (HNF), Forschungszentrum Jülich. This chapter will give an introduction to the most important nanofabrication technologies used in my work and the measurement set-up. The first part of this chapter gives the overview of processes for Si NW FET fabrication technology, including electron beam lithography (EBL), nanoimprint lithography (NIL) and chemical etching. In the second part, the electrical measurement setup and the low frequency noise measurement setup will be described.

3.1 Nanofabrication Techniques

In this work, a novel "top-down" approach for fabrication of Si NW biosensors has been developed. It is based on a combination of nanoimprint lithography and electron beam lithography as well as wet anisotropic etching of Si on a SOI wafer. In this part, the main techniques which were used in this PhD project are described.

3.1.1 Electron Beam Lithography

EBL is widely used to achieve high-resolution patterns in nanotechnology [61-64]. The main purpose of the EBL is similar to the optical lithography: to transfer the defined structure pattern to the substrate with nanometer resolution.

In optical lithography, the structures on the mask are directly transferred to the wafer by the light projection through the mask. The ability to project a clear image of a small structure onto the wafer is limited by the wavelength of the light which is used. Current state-of-the-art photolithography tools use deep ultraviolet (DUV) light with wavelengths of 193 nm and have introduced the use of immersion lithography. This allows fabrication of structures with minimum feature sizes down to 32 nm [65].

In EBL, the structure patterns are directly written to the substrate by the focused electron beam. During the writing procedure, the sample is covered with electron beam resist and then selectively exposed to the electron beam. The electrons accumulate in the areas written, causing a change in the chemical properties of the e-beam resist layer. In this way, the structures are directly defined after development. This form of maskless lithography is widely used to produce the masks used in photolithography, low-volume production of semiconductor components, and structures fabricated for research & development.

However, the resolution of EBL is limited by an effect called the proximity effect [61] of electron scattering in the resist and substrate, which leads to an undesired change in the properties of the regions adjacent to those exposed by the electron beam. Furthermore, its applicability to insulating substrates is often limited by surface charging effects [66]. Unlike patterning on conducting substrates that dissipate excess charge as the beam passes through

the resist, charge is trapped near the surface when the substrate is insulating. This charging causes an unbalanced surface potential of the resist that deflects the beam and causes severe pattern distortion.

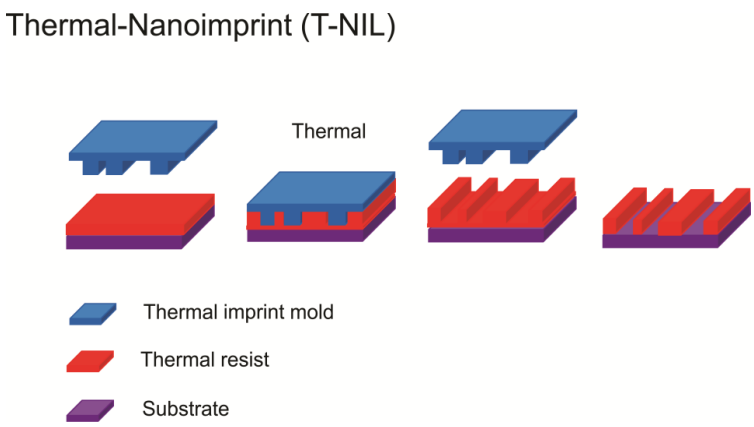
In this work, the nanoimprint mold and some chips with short nanowire were fabricated using EBL, the detailed information were described in the next chapter.

3.1.2 Nanoimprint Lithography

NIL is a simple nanolithography process with low cost, high throughput and high-resolution. In this process, a surface pattern from a stamp is replicated in an imprint resist on the substrate by mechanical deformation. The imprint resist is typically a layer of polymer that is cured later by heat or UV light during the imprinting under pressure [67]. NIL doesn't have the diffraction limit in structure resolution, like we have described in optical lithography, as well as it does not suffer from the proximity effect and charging effect seen in EBL.

The nanoimprint process has been applied for high throughput fabrication of a wide range of nano devices, such as electronic and photonic devices [68, 69], as well as for structuring patterns for biological applications [70]. In 2003, the International Technology Roadmap for Semiconductors (ITRS) included NIL as one of the next-generation lithography candidates for 32 nm technology and as a candidate for 22 nm technology in the roadmap released for 2009 [71]. The mechanism and relevant parameters of this technique have been studied in detail in the last 15 years of NIL development [67, 71, 72].

There are many different types of NIL, but two of them are most known and widespread: thermal nanoimprint lithography (T-NIL) and UV nanoimprint lithography (UV-NIL). The mains steps of these technologies are shown in Figure 3.1.



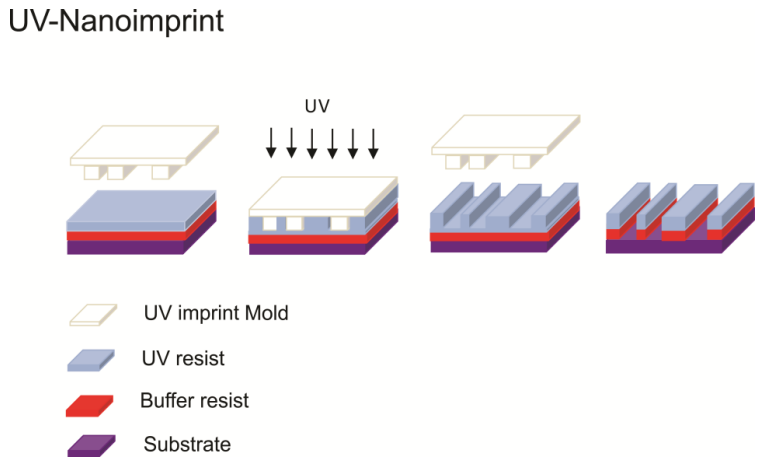


Figure 3.1 Illustration of the main steps in T-NIL and UV-NIL processes.

T-NIL is the first method of NIL, which was developed in Prof. Stephen Chou's group in 1995 [73, 74]. In a standard T-NIL process, a thin layer of imprint resist (thermoplastic polymer) is spin coated onto the sample substrate. Then the mold, which has predefined patterns, is brought into contact with the sample and they are pressed together under certain pressure. When heated up above the glass transition temperature of the polymer, the pattern on the mold is pressed into the softened polymer film. After cooling down, the mold is separated from the sample and the patterned resist is left on the substrate. A pattern transfer process (reactive ion etching, normally) can be used to transfer the pattern in the resist to the material underneath.

UV-NIL was introduced by Haisma and coworkers [75] in Philips Research Laboratories. In this case, a UV curable liquid resist is spin-coated onto the sample substrate and the mold is normally made of transparent material like fused silica. After the mold and the substrate are pressed together, the resist is cured in UV light and it becomes solid. After mold separation, a pattern transfer process can be used to transfer the pattern of the resist into the material underneath.

In this work, T-NIL was successfully used to fabricate the Si NW FET transistors. In addition, UV nanoimprint lithography was also tested in order to compare these two techniques.

3.1.3 Anisotropic Si Etching Using TMAH and KOH

In order to avoid RIE of the active silicon layer, which degrades the device performance [26]. TMAH (tetramethylammonium hydroxide) was chosen to etch the Si layer, as it is very selective for Si against SiO_2 and provides anisotropic etching [23]. During the TMAH etching, the etching rate of Si (111) planes are about 100 times more slowly than all other planes [76]. Lui et al. [48] has shown excellent electronic properties of a nano-FET device fabricated by EBL and subsequent etched by TMAH. The principle of the TMAH etching process of Si on a SOI

(100) wafer is shown in Figure 3.2. A thin layer of silicon dioxide (Figure 3.2 a) or silicon nitride on top of the Si layer acts as a hard mask to protect the Si layer underneath. The TMAH solution etches the exposed Si layer. Due to that all other planes are etched much faster than the (111) plane in combination with the etch stop layer of the BOX, the anisotropic Si etching process creates a (111) plane sidewall which has an angle of 54.47° to the (100) plane. The resulting Si NW has a trapezoidal cross-section (Figure 3.2 b), the defect roughness from the SiO_2 mask layer are eliminated. Therefore, Si NWs with very smooth surfaces compared to the dry etching by RIE can be fabricated using this method.

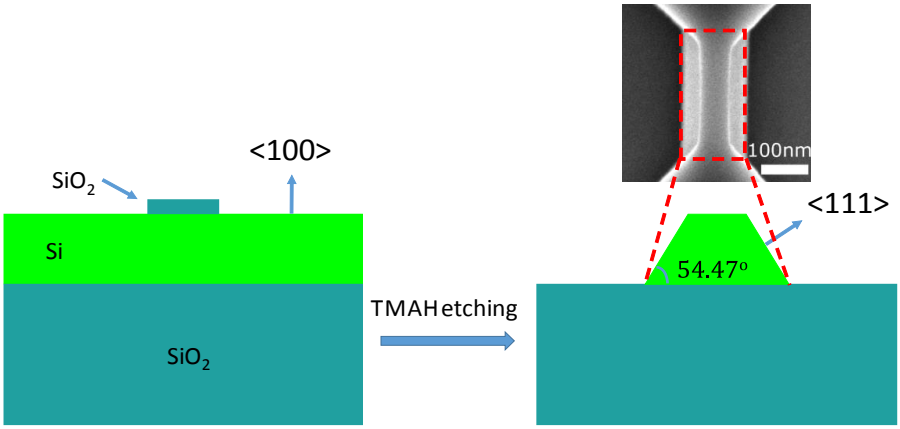


Figure 3.2 Schematics of the anisotropic TMAH etching process of Si on insulator for fabrication of Si NWs. The left is the starting wafer with SiO_2 as the etching mask, the right is the profile of the SOI wafer with Si NW after TMAH etching after hard mask removal. The inset shows the SEM image of Si NW with trapezoidal cross-section.

In order to increase the selectivity of Si (100)/(111)chemical etching. KOH was employed to fabricate the nanoimprint mold. In Table 3.1 we give R_{100} and R_{111}, the etching rates of KOH and TMAH, corresponding to the (100) face and the (111) face, respectively. As we can see, KOH provides much better selectivity. Though KOH etchant provides high selectivity, but it can contaminate Si NWs with metal ions. In order to ensure that the Si NWs remain pure, Si NWs are fabricated by TMAH etching in order to avoid metal ion contamination. In the case of the nanoimprint mold, there is less concern for metal contamination. Therefore, we could use the KOH etching procedure to generate imprint molds, even though it contains metal ions.

Table 3.1 Comparison of anisotropic etching rate and selectivity results between different chemical etchant [77].

Etchant	Operating temperature (°C)	R_{100} (μm/min)	$S=R_{100}/R_{111}$	Mask materials
Potassium hydroxide/ Isopropyl alcohol (KOH/IPA)	50	1.0	400	Si_3N_4, SiO_2 (etches at 2.8 nm/min)
Tetramethylammonium hydroxide (TMAH)	80	0.6	37	Si_3N_4, SiO_2

3.2 Characterization Methods

3.2.1 Electrical Measurements

Electrical properties of Si NW FETs can be determined by measurements of the transfer characteristics and the output characteristics of the devices at room temperature. The transfer characteristics show the drain current, I_{DS}, of the Si NW as a function of the gate-source voltage, V_{GS}, at constant drain-source voltages, V_{DS}. The output characteristics show I_{DS} as a function of the V_{DS} at constant V_{GS}.

As it can be seen in Figure 3.3, the Si NWs are surrounded by dielectric layers, such as a BOX and the top dielectric layer. In this work, the top dielectric layer is either SiO_2 or, in some cases, a stack of SiO_2 and Al_2O_3 layer, that isolate the Si NW from the electrolyte. A BOX layer (145 nm) separates the Si NW from the handle wafer. Hence, the concentration of charge carriers in the NW can be controlled by an electric potential that can either be applied from the top liquid gate, the so-called front gate (V_{FG}), through the thin oxide layer or from the bottom, the so-called back gate (V_{BG}), through the thick BOX layer.

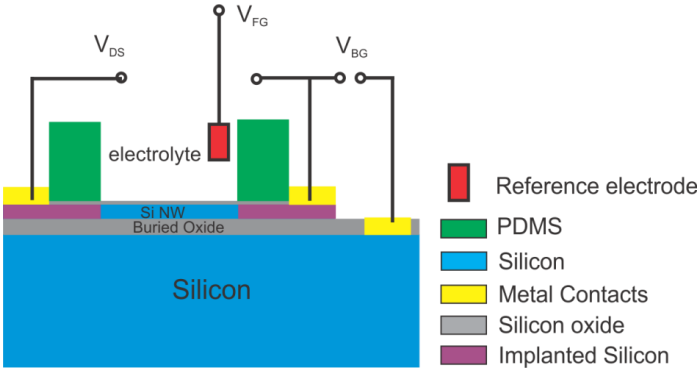


Figure 3.3 Schematic illustration of the device connections for the characterization of the Si NW sensor arrays. A characterization using the back-gate can be done by applying the voltage through the Si substrate with the BOX layer as gate oxide. The front-gate characterization is done by applying the voltage through the reference electrode immersed into an electrolyte solution.

For the front-gate characterization, a reference electrode (silver-silver chloride sintered bare sensor electrodes, in Vivo Metric, USA) was used for all the front-gate measurements in this thesis. The characterization measurements were performed in PBS (0.01 mM) as the electrolyte. The back gate characterization was carried out with the front oxide exposed to air.

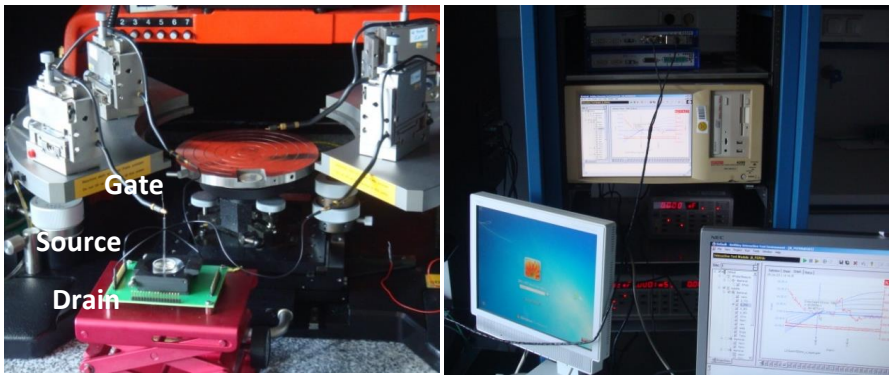


Figure 3.4 Photographs of the measurement setup based on the Keithley 4200 SCM. The encapsulated chip is placed in a socket (see left image) and connected to the Keithley 4200 SCM (see right image). The source, drain, back gate and front gate are connected to the Keithley 4200 SCM by coaxial cables.

Figure 3.4 shows the measurement setup, which uses a commercial Keithley semiconductor characterization system (Keithley 4200 SCM). It has three source measurement units (SMUs) with variable potential and one that is connected to ground. The encapsulated chips were placed in the socket and connected to the system: the common source was connected to ground, the drain, front gate and back gate were connected to the SMU 1, SMU 2, and SMU 3, respectively.

3.2.2 Home-made Noise Measurement Setup

Measuring of low-frequency noise is a complex task since the signal to be measured is very small. This demands the design of a setup with minimized internal noise, as well as avoiding external disturbances from surrounding signals, which may corrupt the measurement. By using batteries as power sources to bias the circuit, one can avoid disturbances from the power grid being injected into the circuit. Also, shielding is important to prevent unavoidable disturbances in the environment from interfering with the measurements. Electrical equipment connected to the grid power may give disturbances at 50 Hz or 60 Hz and the resonant multiples of those frequencies. Wireless units, mobile phones, radio transmitters, etc. provide disturbances in the MHz and GHz range. These signals are outside the bandwidth of the amplifier and the frequency range of interest for the measurements, but these signals may produce an aliasing effect and therefore, the signal is filtered to the necessary bandwidth [77].

The measurements are usually performed in the frequency domain by measuring the power spectral density with a spectrum analyzer. Time domain analysis, with the help of an oscilloscope, is a valuable tool to check the presence of the RTS noise and to have an overview of the signal behavior. A low-noise preamplifier is used to amplify the weak noise signal in order for the signal to be studied with the spectrum analyzer or oscilloscope.

The low-frequency noise characterization of a device is a sensitive tool to study the device performance, especially the characteristics of traps, defects and lattice damage. Consequently, important information about reliability and the current transport can be obtained from low frequency noise studies.

The measurement setup that was used for noise characterization in our work is shown schematically in Figure 3.5. A battery is used to apply voltage to the sample, which can be controlled using a variable resistor from 0 to 1 kΩ. The sample is connected to the power source in series with the load resistance, R_{load}. The resistance can be changed in the range from 1 Ω to 1 MΩ. Such a circuit allows control of the bias voltage from 0 to 6.3 V and specification of the measurement regime.

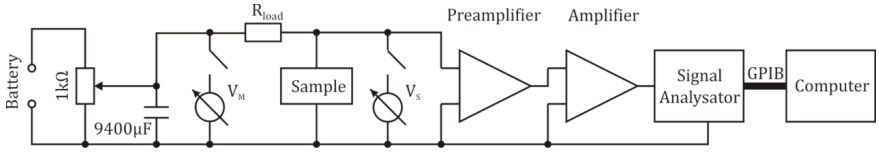


Figure 3.5 The schematic diagram of noise measurement setup [77].

The multimeters V_S and V_M allow one to measure voltages V_{sample} and V_{main}, on the sample and on the whole circuit, respectively. After voltage measurement at these points, DC current can be calculated as $I_S = (V_M - V_S)/R_{load}$. The application of the DC voltage to the sample is necessary for specifying the working point of the device being measured and for measurements of signal fluctuations, such as shot, GR, RTS and flicker noise components. The multimeters are connected to the measurement setup before and after noise measurements to determine the current and voltage applied to the sample, and to check the stability of the system during the noise measurements. During the measurement, multimeters had been disconnected to avoid the influence of their intrinsic noise on the whole noise spectra, the scheme was optimized using one multimeter for measurements of V_S and V_M voltages by switching it to V_S using a relay, and keeping this multimeter at the V_M position during the noise measurements.

The equivalent AC scheme of the measurement part of noise measurement setup is shown in Figure 3.6. Here, R_{sample} is the differential resistance of the sample. It is obtained experimentally from measured *I-V* characteristics. The variable resistance of 1 kΩ and capacitance of 9400 μF, taken together have a negligible influence on the total impedance of the scheme (< 4.2 Ω at frequencies > 1Hz for AC measurements). The parasitic capacitance, C_p, can lead to decay of the measured noise spectra in the high-frequency range, depending on the selected load resistance and the differential resistance of the sample, $R_{Sample} = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)_{V_{GS}=const}$.

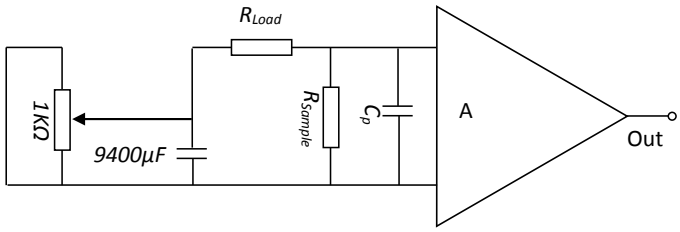


Figure 3.6 Equivalent AC scheme of the circuit connected to the preamplifier part of the measurement setup.

The noise equivalent circuit is shown in Figure 3.7. The sample and load resistances are treated as ideal resistors with current noise sources connected to them.

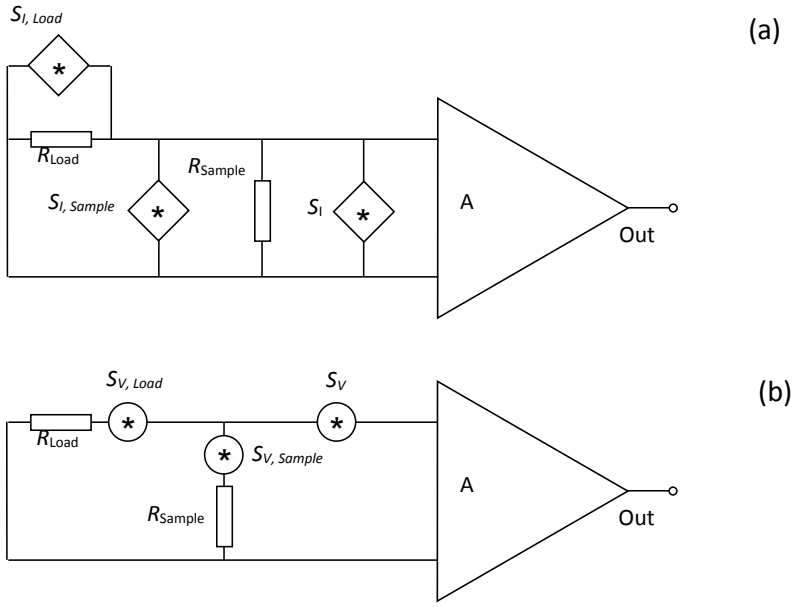


Figure 3.7 Noise equivalent circuit of in parallel with a noise current generator (a) and in series with a noise voltage generator (b) from the schema of Figure 3.6.

where $S_{I,sample}$, $S_{I,load}$ and S_V is the voltage power density of the sample, R_{load} and R_{total}. $S_{I,sample}$, $S_{I,load}$ and S_I are the current power density of the sample, R_{load} and R_{total} respectively. As

$$R_{total} = \frac{R_{load} \cdot R_{sample}}{R_{load} + R_{sample}}. \tag{3.1}$$

Assuming that the voltage fluctuation of R_{sample}, R_{load} equal ΔV_{sample}, ΔV_{load}, the output voltage fluctuation can be written as:

$$\Delta V = \frac{R_{load} \cdot \Delta V_{sample}}{R_{sample} + R_{load}} + \frac{R_{sample} \cdot \Delta V_{load}}{R_{sample} + R_{load}} \tag{3.2}$$

From Equation (3.1), one can rewrite Equation (3.2) to get:

$$\Delta V = \frac{\Delta V_{sample} \cdot R_{total}}{R_{sample}} + \frac{\Delta V_{load} \cdot R_{total}}{R_{load}} \tag{3.3}$$

The voltage noise powers are then given as:

$$S_V = \left(\frac{R_{total}}{R_{sample}}\right)^2 S_{V,\ sample} + \left(\frac{R_{total}}{R_{load}}\right)^2 S_{V,\ Load} \tag{3.4}$$

Our setup allows us to measure the voltage noise power spectral density, S_V. For the analysis of noise it is preferable to use current noise power spectral density, S_I, and the normalized current noise power spectral density multiplied by frequency, S_I/I^2. The S_I relates to S_V as follows:

$$S_I = \frac{S_V}{R_{total}^2} \tag{3.5}$$

The current noise power spectral density is then given as:

$$S_I = \left(\frac{1}{R_{sample}}\right)^2 S_{V,\ sample} + \left(\frac{1}{R_{load}}\right)^2 S_{V,\ Load} \tag{3.6}$$

As $S_{V,\ Load}$ is only thermal noise, and if $S_{V,\ sample} \gg S_{V,\ Load}$, or $R_{sample} \ll R_{Load}$ at low frequencies, then $S_{I,\ sample} \approx S_I$. Therefore, in order to monitor the RTS noise, we choose ten times higher R_{load} than R_{sample} during the RTS measurements.

The amplified AC signal from the sample goes to the input of a dynamic signal analyzer HP35670A, which measures voltage fluctuations and, using fast Fourier transform, calculates the Voltage noise spectrum S_V of the device.

The home-made noise measurement setup was used in this work. The samples under investigation have to be placed in the steel box or in the vacuum chamber. The turbomolecular pump together with a mechanical pump allows the setup to obtain the vacuum down to 10^{-5} mBar in the chamber. The measurements of noise spectra at different temperatures were performed using a stirling cooler, which allows the user to decrease the temperature down to 60K at the copper finger inside the vacuum chamber. The sample under investigation is connected through dampened vibration cooper sheets to the finger. The temperature on the

sample is controlled by a silicon diode temperature sensor. All circuits with their batteries are placed inside of the steel box to avoid additional noise disturbances from outside. The temperature monitor, temperature controller, multimeter and spectrum analyzer are connected to the computer through GPIB and COM interfaces to measure the noise spectra in a fully automated process.

To automate the setup the program code Get Noise Spectrum v8 was developed using HT Basic [77].

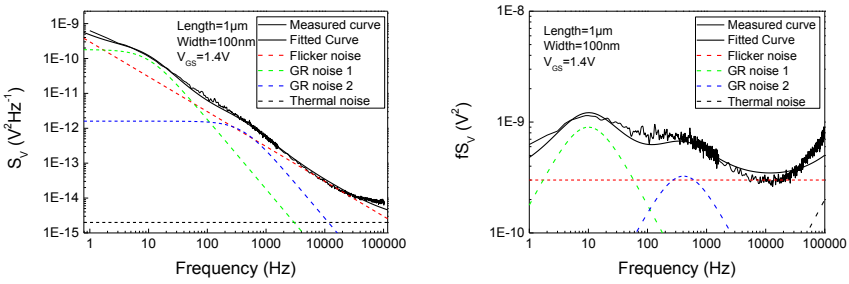


Figure 3.8 (a) Typical measured noise spectra of a Si NW FET represented as the frequency dependent voltage noise power spectral density. (b) Multiplied by the frequency, *f*, voltage noise power spectral density from (a) as a function of frequency to obtain the characteristic frequency for each of the G-R noise components in the spectra.

Typical noise spectra measured in the first range from 1 Hz to 1600 Hz with 1 Hz steps and in the second range from 64 Hz to 102 kHz with 64 Hz step are shown in Figure 3.8 (a). The measured noise spectra are usually composed of thermal, flicker and GR noise components. These components can be separated in the whole range of the measured noise spectrum. The example of such a separation is demonstrated in Figure 3.8. To distinguish noise components, it is convenient to multiply the density shown in Figure 3.8 (a) by frequency, as it is shown on Figure 3.8 (b). Here, several bumps denote the G-R noise components, while the flicker noise component will be almost horizontal as a result of multiplication by frequency.

4. Si NW FETs Fabrication

In this thesis, a novel "top-down" approach was developed to fabricate Si NW FET biosensors. This approach is based on the combination of NIL and wet anisotropic etching.

Four different kinds of Si NW FET samples were fabricated:

- Back gate Si NW FETs (3×3 mm^2) fabricated by NIL with channel length in micrometer range.
- Back gate Si NW FETs (3×3 mm^2) fabricated by NIL with channel length in submicrometer range.
- Si NW FET biosensors (5×5 mm^2) fabricated by NIL with channel length in micrometer range.
- Si NW FET biosensors (3×3 mm^2) fabricated by EBL with channel length in submicrometer range.

The following paragraphs in this chapter will firstly discuss the NIL technology including fabrication of imprint mold and the optimization of T-NIL for Si NW structure fabrication. Next, the design and fabrication steps of our four kinds of devices will be given.

4.1 Nanoimprint Lithography

NIL is a promising technique for transferring images from an imprint stamp to a resist in which the images are replicated. Unlike current state-of-the-art photolithographic processes which require very expensive process equipment to make masks and to expose a photoresist material with an image on the mask, NIL combines the advantages of high-resolution with low costs and high throughput. NIL is a promising technique for obtaining nano-size patterns (as small as a few tens of nanometers or less) in a media. Although an imprint stamp can be made to imprint features of any size, imprint stamps with features that are nanometer sized or smaller are of particular interest because of a need to imprint features that are smaller than a lithography limit of currently used optical photolithography processes and at a lower cost.

The resolution of imprint lithography is largely limited by the resolution of the imprint mold. EBL and RIE are employed to make mold with high resolution. However, the current technology of mold fabrication is suffering from a lot of problems.

The first is related to the mold's edge roughness, which is a very important feature for NIL because it determines the quality of the replicated structure. Reducing edge roughness during EBL is time-consuming or expensive because it requires smaller beam step size and hence results in longer writing time or increasing energy of the electrons for higher resolution. The second important limitation is that the vertical and smooth sidewall profile of the mold is very important in obtaining a smaller demolding force, but it is difficult to obtain exactly vertical and smooth sidewalls by using dry etching because the resist layer with edge roughness is

projected onto the mold layer as well as the interaction processes with the mask layer during dry etching. Accordingly, there is a need for developing of a technology for fabricating of high smoothness nanostructures of mold, which can be used for NIL.

Additionally, UV-NIL attracts much interest as it works at room temperature and cured under UV light. It can allow avoiding the expanding at high temperature compared with T-NIL. However, the quartz, which is the normal substrate material used as the mold, can be anisotropic etched only using dry etching process.

In this work, in order to fabricate Si NW FETs using T-NIL, the imprint mold was fabricated by chemical etching instead of the conventional dry etching method. Also fabrication of UV-NIL mold using dry etching was described.

4.1.1 Nanoimprint Mold Fabrication

In a standard T-NIL process, a thin layer of imprint resist (thermoplastic polymer) is spin coated onto the sample substrate. Then the mold, which has predefined patterns, is brought into contact with the sample and they are pressed together under certain pressure. When heated up above the glass transition temperature of the polymer, the pattern on the mold is pressed into the softened polymer film. After cooling down, the mold is separated from the sample and the pattern resist is left on the substrate. A pattern transfer process (RIE, normally) can be used to transfer the pattern in the resist to the underneath substrate.

UV-NIL, a UV curable liquid resist is spin coated onto the substrate and the mold is normally made of transparent material like fused silica. After the mold and the substrate are pressed together, the resist is cured in UV light and becomes solid. After mold separation, a similar pattern transfer process can be used to transfer the pattern in resist onto the underneath substrate.

In this thesis, two kinds of molds were fabricated, they are used for T-NIL and UV-NIL. The fabrication process of two different nanoimprint molds are totally different.

4.1.1.1 T-NIL Mold

The mold fabrication process is schematically shown in Figure 4.1. Firstly the Si wafer with 110 orientation is chosen as the starting wafer, then a 120 nm of oxide layer was grown on the surface using dry thermal oxidation, next the negative and inverse structure was defined by EBL on the spin coated PMMA 669.04 resist. The e-beam writing was done using a Leica EBPG 5000 Plus. The EBL parameters used for coarse and fine patterns are listed in Table 4.1. Afterwards, RIE etching was used to transfer the structures to the SiO_2 layer, then the sample was dipped into 20% KOH solution at 30 ℃. It resulted in 180 nm depth etching. Before this wet etching, the residual SiO_2 was removed using 1% HF etching for 20 seconds. After KOH etching, the sample was dipped into buffered HF (BHF) (875-125) solution to etch the SiO_2 layer, 180 nm depth mold with very smooth surface was obtained.

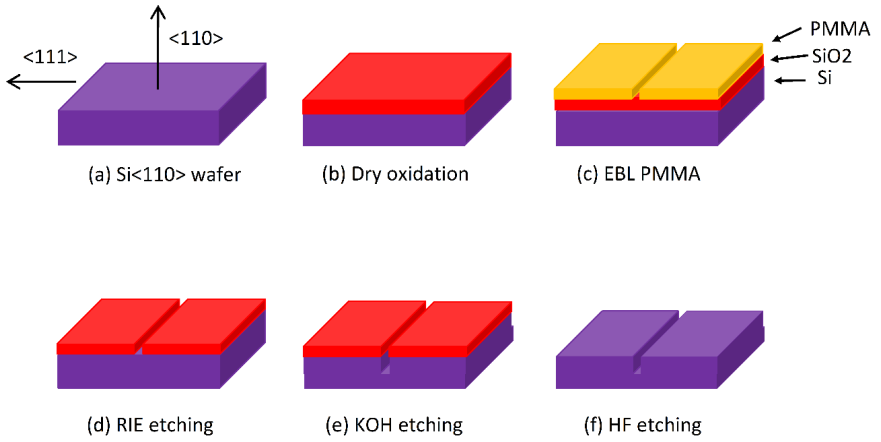


Figure 4.1 Schematic process of mold fabrication using wet chemical KOH etching [78].

Table 4.1 The e-beam lithography parameters used for fabrication of the NIL mold.

Patterns	E-beam parameter		
	Dose(μC/cm^2)	E-beam current (nA)	Beam step size (nm)
Conducting pads (coarse pattern)	225	150	50
Nanogrooves (fine pattern)	380	0.1	5

To enhance the release of substrate and mold after an imprint process it was necessary to evaporate an anti-adhesion layer on the mold, which was exposed to the vapour of Trichloro(1H,1H,2H,2H-perfluorooctyl)silane (FOTS) in order to form a monolayer of fluorsilane (anti-sticking layer) and reduce the surface energy.

Due to novel chemical etching method, very smooth surface of the mold were obtained. Figure 4.2 (a) shows the SEM image of imprint mold fabricated using chemical etching, Figure 4.2 (b) shows one of the nano groove, this is the key component of imprint mold, we can find that after chemical etching, we can get vertical sidewall with low edge roughness along (111) faces. Figure 4.2 (c) and (d) shows the 3D and 2D AFM pictures of the imprint mold. These results demonstrate that the surface and the bottom of the mold are very smooth which is a very important metric for mold application during NIL process.

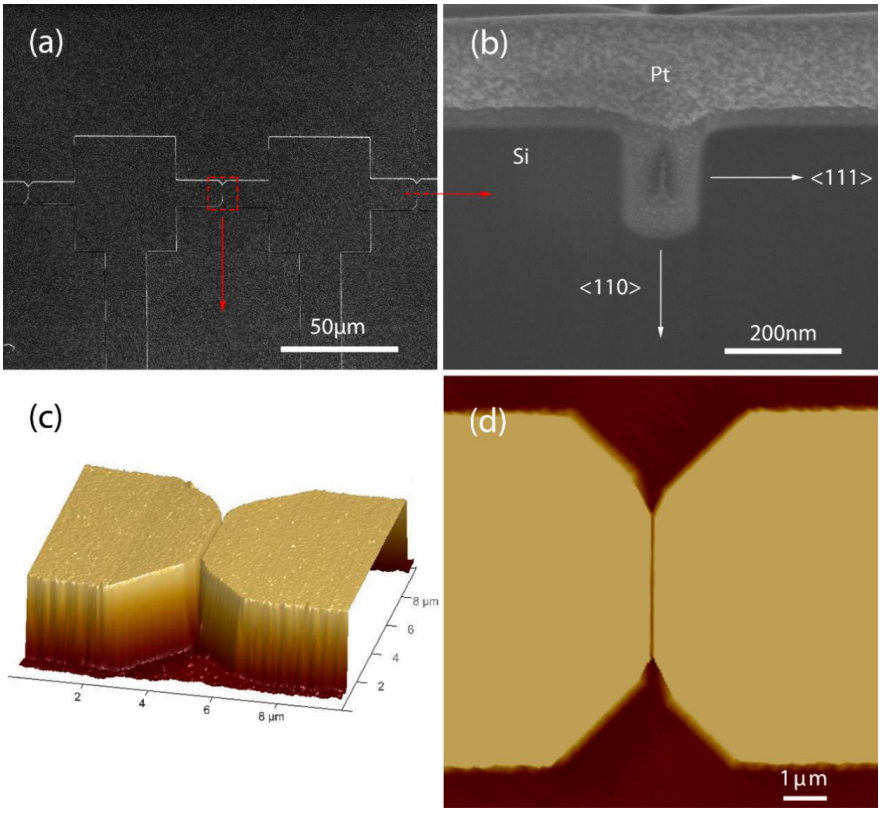


Figure 4.2 Surface characterizations of an imprint mold fabricated using KOH etching: (a) SEM image of a mold. The red square indicates a single nanogroove. (b) FIB cross section of the nanogroove of the mold. The dimensions of nanogroove cross section are following: height is 220 nm, width is 135 nm. 3D (c) and 2D (d) AFM images of the nanogroove in the fabricated imprint mold [78].

In order to investigate the material etching of different orientations for mold fabrication, we designed many NWs along different orientations of the Si wafer. Figure 4.3 (a) and (b) show results of the anisotropically etching along <111> face. It should be noted, that the etching rate is much lower for <111> face among all of the faces. This results in smooth and vertical sidewall. However, Figure 4.3 (c) and (d) show the etched nanogrooves oriented along the <111> direction, which is perpendicular to the (111) planes, have coarse and sloped planes. These results further confirm that the chemical etching procedure used is highly anisotropic.

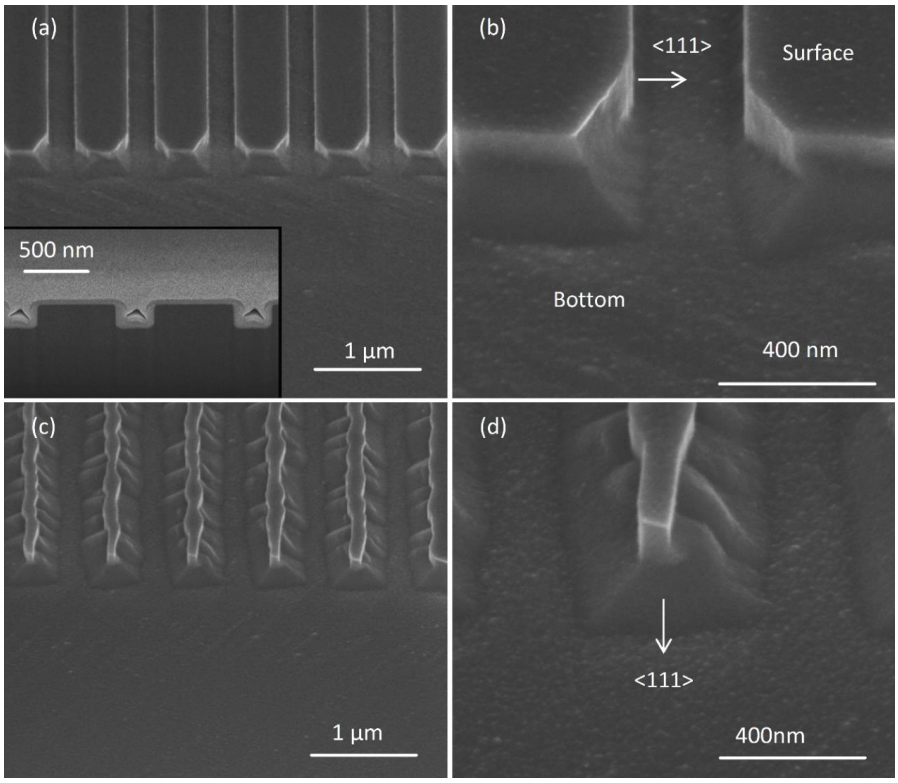


Figure 4.3 SEM image of a nanoimprint mold with nanogroove arrays along different directions fabricated using KOH etching. (a) SEM image of nanogroove arrays aligned along (111) planes. The inset shows the FIB cross section of the obtained mold. (b) Zoomed single nanogroove from the SEM image of (a). (c) SEM image of nanogroove arrays aligned perpendicular to (111) planes. (d) Magnified SEM image from (c) [78].

4.1.1.2 UV-NIL Mold

UV-NIL has attracted a lot of interests compared with T-NIL because the advantage of room temperature processing.

In general, nanoimprint mold fabrication using EBL is easier for conducting substrates than insulating ones, because the charging effects related to the lack of charge dissipation can be avoided. As transparent substrates are needed for UV NIL, stamps are almost exclusively made out of quartz or fused silica which are nonconducting. Because of this reason, the use of charge dissipation layers is necessary.

The mold fabrication process is summarized in Figure 4.4. The starting material is a quartz substrate (step 1), on which 180 nm PMMA spin coated on the substrate (step 2). Afterwards, a 20 nm-thick chrome layer is deposited by evaporation (step 3). Chrome was chosen because it is a conductive material that can drive away the charges during the EBL step and it has a high etching selectivity with respect to silicon dioxide and PMMA resist. EBL (step 4) is performed to pattern on the same wafer with micro- and nano-scale features. The electron beam writing parameters are shown in Table 4.2. After Electron beam writing, the chrome is

etched by ceric ammonium nitrate. Followed development was performed and the structure will appear. RIE was used to etch quartz as well as with the PMMA as a hard mask (step 5). The etching time was chosen according to the required mold depth and the etching rate. At last, the resist is stripped by O_2 plasma (step 6).

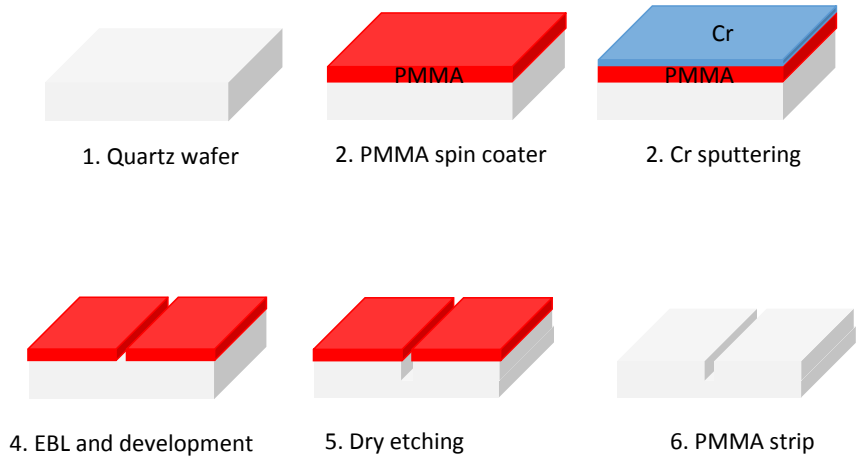


Figure 4.4 Schematic process of mold fabrication for UV-nanoimprint lithography.

Table 4.2 The e-beam writing parameters used for fabrication of the nanoimprint mold.

E-beam parameter	Dose ($\mu C/cm^2$)	E-beam current (nA)	Beam step size (nm)
Conducting lane (Coarse pattern dose)	225	150	50
Nanowire (Fine pattern dose)	380	0.1	5

Once the molds are fabricated (Figure 4.5), they are treated with the vapour of FOTS in order to form a monolayer of fluorsilane to enhance the release of substrate and mold after an imprint process. It is an anti-sticking layer that reduces the surface energy of the mold by depositing a thin layer of fluorocarbon film at its surface.

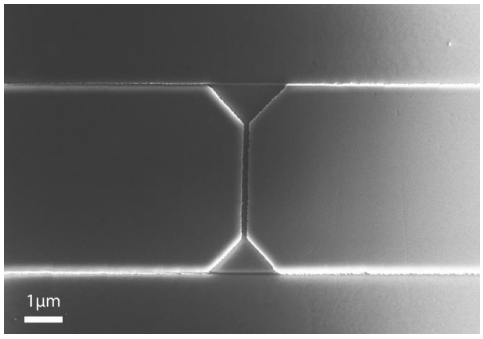


Figure 4.5 Top-view SEM UV nanoimprint mold image.

4.1.2 Optimization of T-NIL

Two mold designs (Figure 4.6 a and b) were used to print our devices, the left one is the old design, the right one is the new design and each cell has the same size of 5 × 5 mm^2.

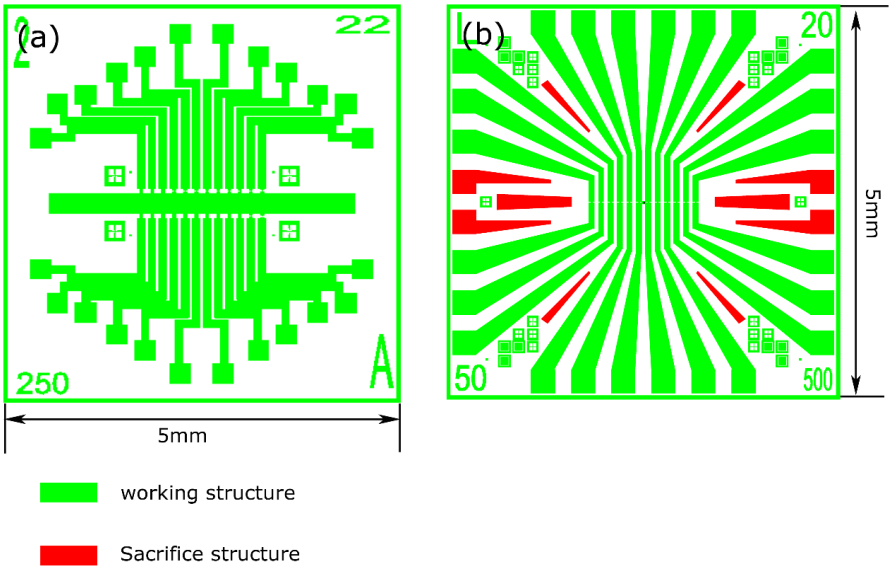


Figure 4.6 Picture of one of the cells from the old design (a) and new design (b). The red color structures in the new design is the sacrifice structures designed to increase the resist distribution.

The nanoimprint processes were performed using two kinds of molds (the designs shown in Figure 4.6) which are 180 nm in depth. An air cushion press process (Nanonex NX2000) was used allowing a compensation of the mold's stiffness by adjusting the imprint pressure. The thermal resists NXR-1025 (Nanonex Corp.) were spin-coated on the substrate and the Large and small structures with widths ranging from 300 µm to 50 nm were created simultaneously from the mold after T-NIL. In order to optimize the imprint work, the quality of T-NIL is studied by variation of different conditions: the resist thickness, imprint temperature, and imprint pressure listed in Table 4.3.

Table 4.3 Results (quantity of the defects) of T-NIL using different design and under different imprint conditions: Rotation speed, Temperature, Pressure.

Designs	Rotation speed, rpm	Temperature/℃	Pressure/Psi	Quantity of the defects
Old design	4000	150	550	16
	4000	200	550	0
	3000	150	200	18
	3000	150	550	0
New design	4000	150	550	15
	4000	200	550	0
	3000	150	200	0
	3000	150	550	0

According to Table 4.3, at 4000 rpm, 550 Psi, 150 ℃, the quantity of the defects from the replicated pattern were 16 and 15 from both designs as shown in Figure 4.7 (a-b) and (c-d), the white arrow indicates the imprint defect. When increase the temperature to 200 ℃, both designs allow printing the good patterns (0 defect). At 3000 rpm, the resist is thicker than 4000 rpm. At 200 psi and 150 ℃, the quantity of the defects from the printed pattern is 18 vs. 0 compared from the old design to the new design. When increasing the pressure to 550 psi, under both conditions, good patterns (0 defect) shown in Figure 4.8 (a-b) and (c-d) can be printed.

These results indicate that, because of the viscous polymer flow, larger features on the mold have to displace more polymer material over larger distances. Thus, patterns with large features are much more difficult to be printed than nanpatterns. That is why we can find the defects in the large patterns shown in Figure 4.7 (c) and (d). However, increasing the temperature, pressure and thickness of imprint resist will be helpful for the replication of different patterns. Also the design is important: the optimized design can be helpful for the distribution of the resist more homogeneously, for example, the new design with sacrifice structure has a more uniform structure distribution then the old design (Figure 4.6).

As indicated from the results described before, increasing of the resist thickness and temperature, we can replicate the patterns from both designs successfully, but thick resist and high temperature will be harmful for the T-NIL. For example, when increase the resist thickness, it will decrease the NW dimensions after O_2 isotropically etching of imprint resist. Secondly, imprint resist will be cured under high temperature, this results in problem during

the resist stripping process. Additionally, high temperature will damage some materials, it will limit the T-NIL application.

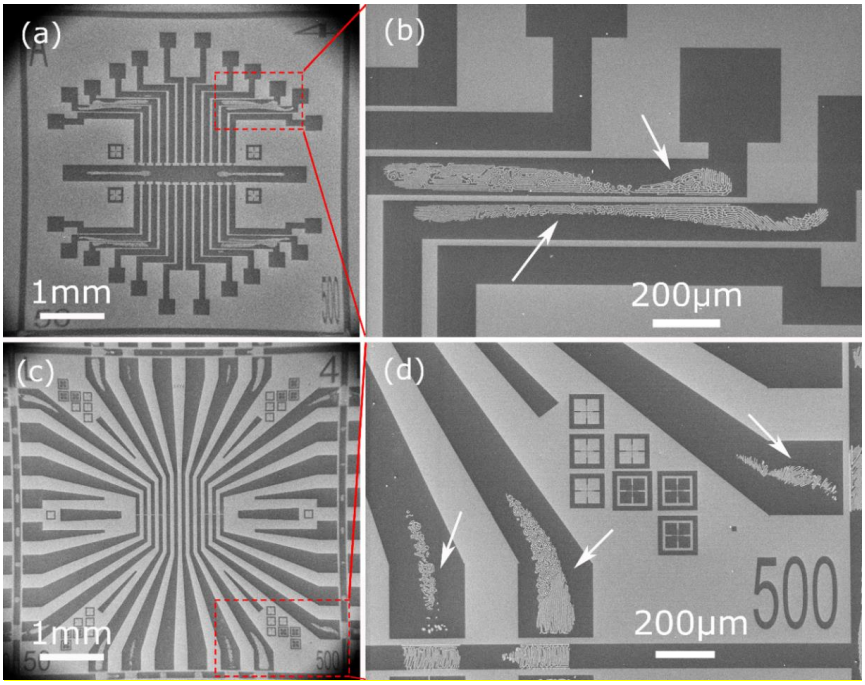


Figure 4.7 SEM images of thermal imprinted chips from old design (a) and new design (c) and its enlarged area SEM images (c) and (d) from the red tangle area at the same imprint conditions: Rotation speed = 4000 rpm, Temperature = 150 ℃, Pressure = 550 psi. The white arrow indicates the imprint defect.

T-NIL under higher pressure condition was demonstrated successful replicating patterns into wafers as shown in Figure 4.8 (a-d) from two designs under the same nanoimprint conditions: 3000 rpm, 550 Psi, 150 °C. The imprinted pattern transferred to SOI wafer after O_2 plasma etching of imprint resist, plasma etching of SiO_2 and TMAH chemical etching of Si as shown in Figure 4.9 and Figure 4.10 from old design and new design, respectively. These results demonstrate that some defects appear in the case of old design, but they are omitted in the case of new design.

In the old design, the same feature height can be achieved for both large-scale and nanoscale patterns under high pressure. However, due to mold bending under high pressure, the area with relief patterns penetrate deeper into the resist layer than the area with dense patterns, leading to a thinner residue layer in the center region than that in the corner region. If the residual in the corner are etched correctly, the structure in the center will be destroyed due to over etching of resist in the center area. However, if the residual in the center are etched correctly, the corner area will be less etched (Figure 4.9), it increase the failure rate of T-NIL. But in new design, we can't find any defect as shown in Figure 4.10. This is due to the optimized patterns as shown in Figure 4.6 (b), sacrifice patterns added in the new design absorb the resist in the empty area, even at high pressure, the mold deformation can be

neglected. This will result in the same height of residual layer, which will be easier for the residual etching. As a result, the large-size structures are successfully replicated in the new design as show in the Figure 4.10.

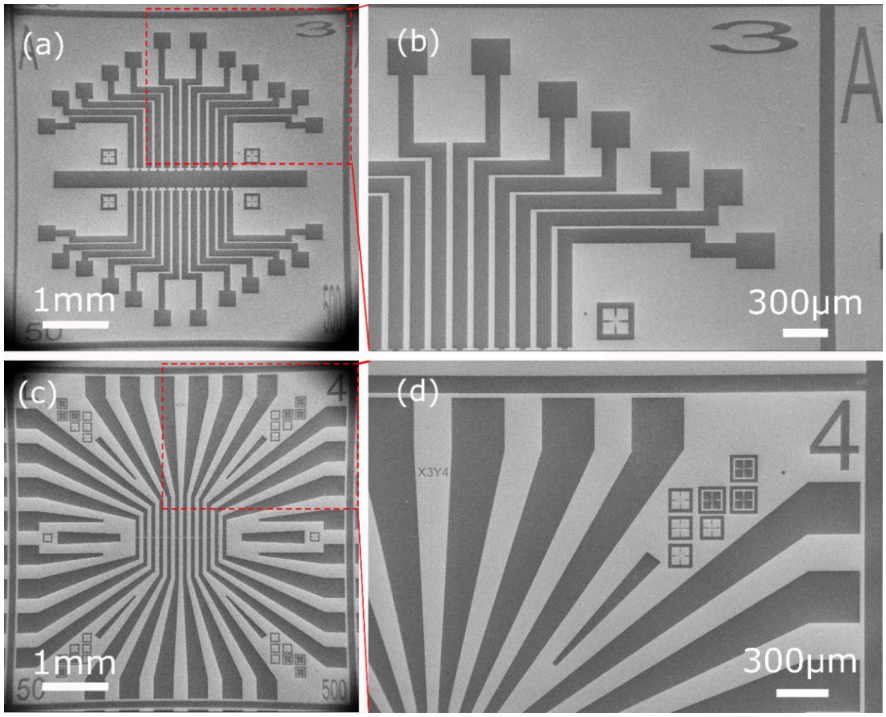


Figure 4.8 SEM images of thermal imprinted chips from old design (a) and new design (c) and its enlarged area SEM images (c) and (d) from the red tangle area at the same conditions: Rotation speed = 3000 rpm, Temperature = 150 ℃, Pressure = 550 psi.

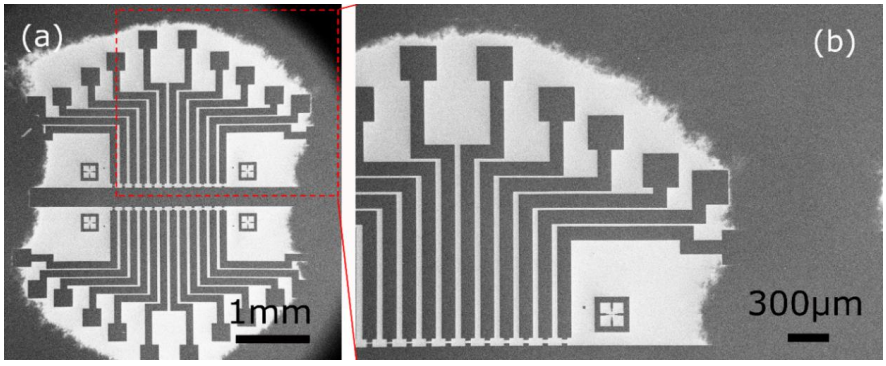


Figure 4.9 SEM image of the center area (a) and in the edge area (b) of the chips fabricated by T-NIL from old design after chemical etching. T-NIL conditions: Rotation speed = 3000 rpm, Temperature = 150 ℃, Pressure = 550 psi.

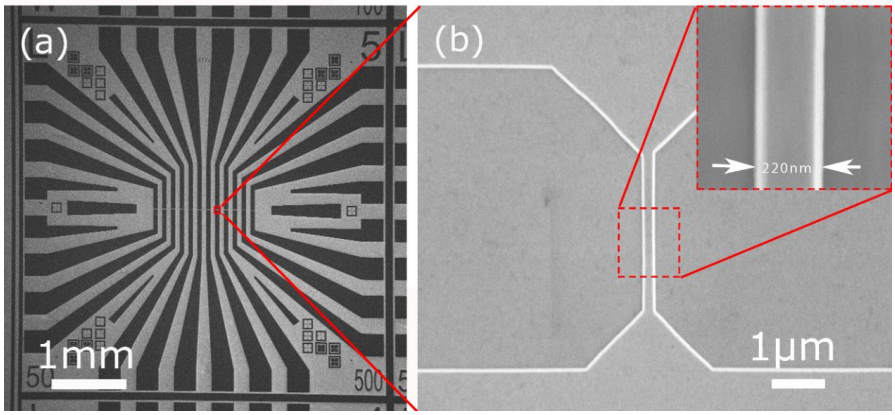


Figure 4.10 (a) SEM image of the chip fabricated by T-NIL from new design after chemical etching. (b) SEM image of Si NW FET with drain, source and NW channel. The inset shows the amplified NW section. T-NIL conditions: Rotation speed = 3000 rpm, Temperature = 150 ℃, Pressure = 550 psi.

In summary, very smooth imprint molds were fabricated by KOH etching instead of traditional dry etching. Adding sacrifice structure to imprint mold can be helpful for patterning large-scale as well as sub-micron size structures. This approach allows avoiding the mold deformation under higher pressure.

4.2 Fabrication of Back Gate Si NW FETs with Micrometer Channels

4.2.1 Chip Design

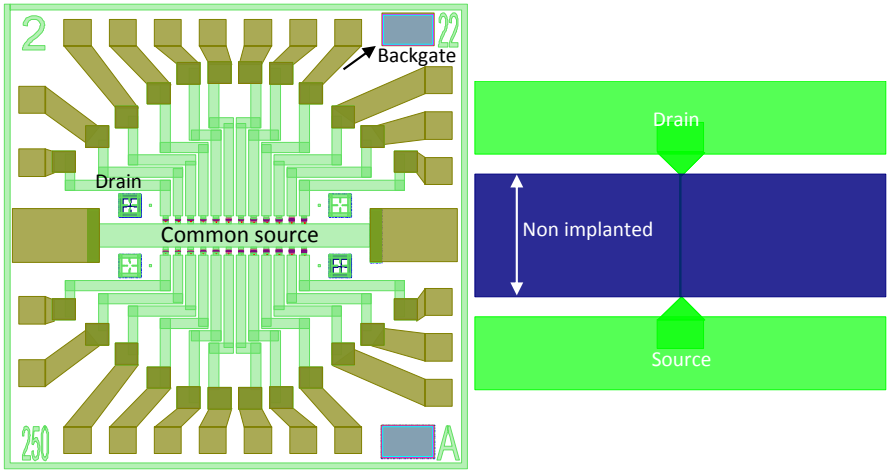


Figure 4.11 Layout (left) of the 12 × 2 Si NW array with 24 drain and one common source and two backgate electrodes. The nanowire area (right) between source and drain contact line.

In the first design of the Si NW chips, two sets of 12 NWs structures with common source were designed. The chip with cell size of 3 × 3 mm^2 is shown in Figure 4.11 (left). The chip cell

included quite long contact lines representing 24 individual drains, a common source contact and the nanowires between the contacts.

There are seven kinds of devices in this design as listed in Table 4.4 (a) and (b). The lengths range from 2 to 22 µm, the width changes from 50 to 500 nm. The source and drain contact lines were highly implanted with boron ions except the nanowire region (Figure 4.11 (right)).

The contact lines and nanowires were fabricated by T-NIL. For a more detailed description refer to Appendix B. 1.

Table 4.4 (a) The designed chips.

Chips Number	Name	Length L/µm												W/nm
10	L=2-22, W=250	2	3	4	6	8	10	12	14	16	18	20	22	250
10	L=2-22, W=500	2	3	4	6	8	10	12	14	16	18	20	22	500
3	L=16-21, W=100	16	17	18	19	20	21	21	20	19	18	17	16	100

Table 4.4 (b) The designed chips.

Chips Number	Name	Width W/nm												L/µm
10	L=3, W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	3
10	L=4, W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	4
10	L=5, W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	5
3	L=20, W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	20

4.2.2 Chip Processing

Figure 4.12 depicts the main fabrication steps for the fabrication of Si NW array FETs from SOI wafer. A SOI wafer with original Si thickness of 70 nm and buried oxide (BOX) layer thickness of 145 nm was used to fabricate these devices. The process started by growth of a 37 nm thin layer of dry oxide on top of the SOI substrate, which was used as a hard mask, followed by the T-NIL to define the contact lines and wire structures. After the T-NIL, dry etching of SiO_2 using RIE and anisotropic etching of Si by TMAH solution were performed. Optical lithography was used to open the backgate and PECVD were employed for the passivation of the devices. The imprint mold, all the masks for optical lithography and the final devices were fabricated at HNF, Forshungszentrum Jülich.

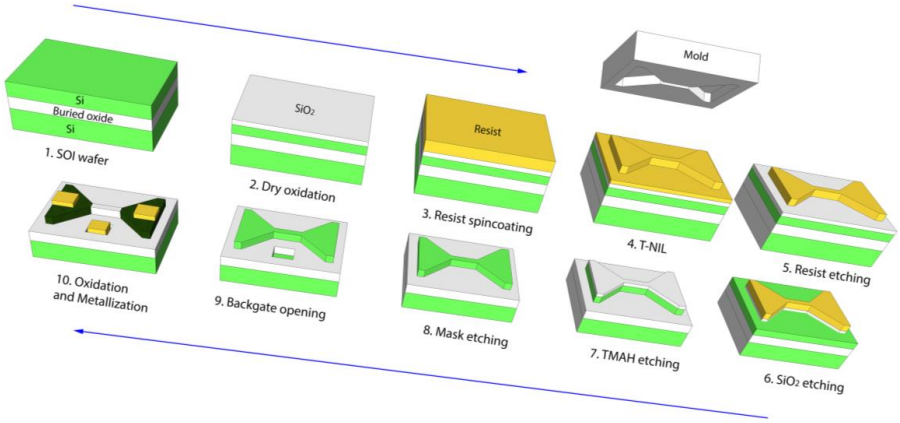


Figure 4.12 Flow of the fabrication steps of Si NW FETs.

In the following, the fabrication steps of the nanowire sensors are described in detail:

SOI wafers purchased from SOITEC, France, were used as a starting material for the process to fabricate these devices (Figure 4.12, step 1).

Thermal oxide was grown as a hard mask layer for the TMAH etch step (step 2). After the oxidation, the top SiO_2 layer is about 37 nm, the Si active layer is about 51 nm.

T-NIL transferred the structures from the mold to the SOI wafer (step 3). The nanoimprint process were performed by using an NX-2000 with air cushion press. The imprint process was performed as described below [31]:

- The nanoimprint resist (Nanonex 1025) was spin coated on the SOI wafer and incubated at 90 °C for 20 min. The thickness of the resists was determined to about 220 nm by ellipsometry.
- The mold was cleaned in acetone with megasonic and dried by Ar-gas. The SOI wafer and the mold were carefully aligned based on the large flat of the wafers and both were fixed by two polyester foils and transferred to the imprint chamber. The alignment has to be performed carefully in order to have reliable devices, because the TMAH etching strongly depends on alignment of the structures with respect to the <110> direction. Before imprinting on the SOI wafers, the imprint was done on a test wafer to remove the small particles on the mold because a small particle may create a large defect on the wafer after the imprint process.
- The imprint chamber was evacuated for 5 minutes to remove air out of the structured cavities. After evacuation, the temperature of the imprint chamber was increased to 140 °C and a pressure of 200 Psi was applied as the pre-imprint process. The main imprint process was carried out at a temperature of 150 °C and a pressure of 550 Psi for 6 minutes. During the main process, the temperature and pressure were kept constant. After the main process, the imprint chamber was cooled down to a venting

temperature of 40 °C, while the pressure was kept at 450 Psi. When the temperature reached the venting temperature, the pressure of the imprint chamber was released. The mold and the substrate were carefully separated by hand at room temperature.

In step 4, the structure of the mold was transferred to the nanoimprint resist after thermal imprinting.

In step 5, the residual resist layer was removed by oxygen plasma. This step is very important in our process. Because the residual should be removed completely and it determined the next steps if performed successfully.

In step 6, the structures were transferred to the SiO_2 layer by RIE. After that, the resist was completely removed by oxygen plasma.

In step 7, the TMAH etching was performed with a 25% TMAH solution, while the temperature was kept at 90 °C during the process. Before the etching in TMAH solution, the wafers were dipped for 20 seconds into 1% HF solution to remove the native oxide. Then they were rinsed in deionized water. The Si was etched down to the BOX layer in about 15 seconds as observed by a change of the wafer color. However to ensure the process and to create Si NWs with smooth edges, the wafers were etched for 30 to 60 seconds and were subsequently rinsed several times in deionized water.

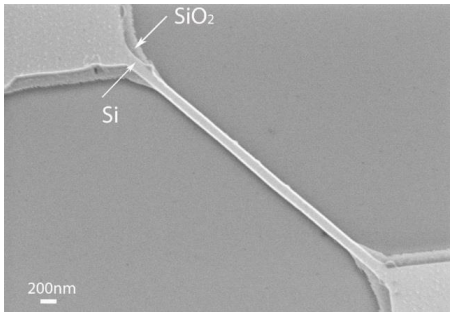


Figure 4.13 NW structure after TMAH etching. The TMAH etching process eliminates the roughness of the top SiO_2 mask layer.

Figure 4.13 shows a Si NW after TMAH etching with the SiO_2 hard mask on top. It can be clearly seen that the roughness at the edges of the SiO_2 hard-mask was not transferred to the Si NW structure during the TMAH etching step. It was found that the TMAH etching resulted in very smooth Si surface although the quality of the SiO_2 mask was not very good.

After the TMAH etching process, the mask layer was completely removed by 1% HF solution as shown in step 8.

Next in step 9, the backgate contact pad was opened using photolithography and HF etching through the buried oxide layer.

Afterwards, thin oxide layer was grown and together with the photoresist defined by photolithography, as a protection mask for the ion-implantation.

In the following implantation step, arsenic ions were implanted on the contact lines to decrease the source and drain serial resistances of the Si NW arrays. The arsenic ions were implanted with a dose of 5×10^{14} cm^{-2} and an energy of 8 keV.

After the ion implantation, the photoresist was removed by acetone, piranha cleaning and subsequently annealed at 950 °C for 30 seconds in the N_2 atmosphere to activate the implanted ions. Then the protection oxide layer was etched by 1% HF solution. A thin layer of dry thermal silicon oxide (6 nm) was grown and then a 100 nm PECVD SiO_2 layer was deposited.

The wafers were then structured by optical lithography and the SiO_2 layer was etched by HF 1% to open source, and drain, and back gate contact pads.

In the last step of the fabrication process, a lift-off process was performed to deposit a stack of metals (150 nm Al, 10 nm Ti, 150 nm Au) on the contact pads.

4.3 Fabrication of Back Gate Si NW FETs with Submicrometer Channels

In order to study RTS signals in Si NW FETs, we designed Si NW FETs with submicrometer channels which were much shorter than the devices described above.

4.3.1 Chip Design

The Si NW chips were mainly based on 12 × 2 arrays of Si NW FETs. The chip cell size was 3 × 3 mm^2 as shown in Figure 4.14 (left). The chip cell included quite long contact lines of 24 individual drains and a common source contact to the nanowires. The individual NW is shown in Figure 4.14 (right).

There are five kinds of devices in this design as shown in Table 4.5 (a) and (b), one of them are with the same width of 50 nm and 100 nm, the Length changes from 0.1 μm to 12 μm. Another kind of design includes the structures with the same length of 500 nm and 1 μm, but the width changes from 50 nm to 500 nm.

The contact lines and nanowires were fabricated by T-NIL. The source and drain contact lines were highly implanted with arsenic ions except the nanowire region (Figure 4.14 (right)). The back gate contact to the bulk Si wafer was opened through the BOX layer using photolithography and wet etching. For a more detailed description refer to Appendix B.2.

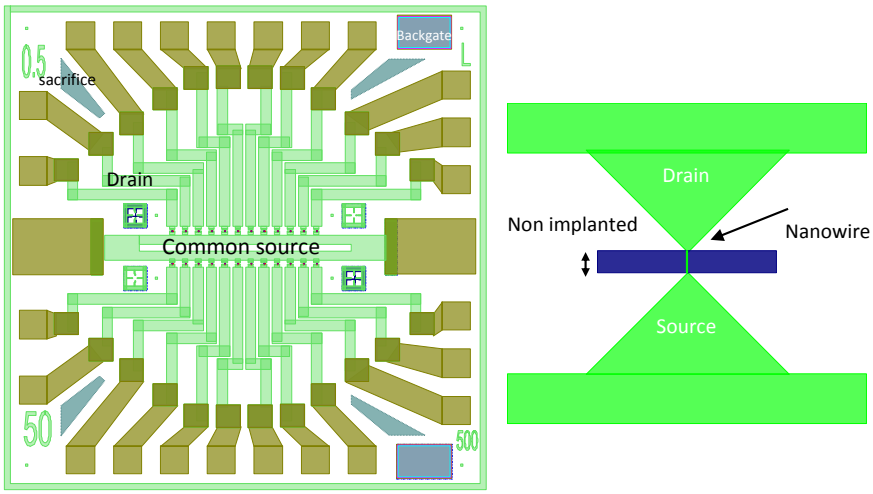


Figure 4.14 Layout (left) of the 12 × 2 Si NW array with 24 drain and one common source and two backgate electrodes. The nanowire area (right) between source and drain contact line.

Table 4.5 (a) The designed chips.

Chips Number	Name	Length L/µm												W/nm
16	L = 0.1-12, W = 50	0.1	0.2	0.4	0.6	0.8	1	2	4	6	8	10	12	50
16	L = 0.1-12, W = 100	0.1	0.2	0.4	0.6	0.8	1	2	4	6	8	10	12	100
8	L = 0.1-0.4, W = 50	0.1	0.1	0.1	0.1	0.2	0.2	0.2	0.2	0.4	0.4	0.4	0.4	50

Table 4.5 (b) The designed chips.

Chips Number	Name	Width W/nm												L/µm
8	L = 0.5, W = 50-500	50	100	150	200	250	500	500	250	200	150	100	50	0.5
8	L = 1, W = 50-500	50	100	150	200	250	500	500	250	200	150	100	50	1

4.3.2 Chip Processing

The fabrication of these devices is the same as the first devices, only some of the steps are different:

- Because our nanowires are too short, it is impossible to define the protection layer by photolithography. Instead of the photolithography, we used the EBL to define the protection pattern on HSQ resist.

Table 4.6 The e-beam lithography parameters used for fabrication of the devices.

E-beam parameter	Dose ($\mu C/cm^2$)	E-beam current (nA)	Beam step size (nm)
protection pattern	1100	1	5

The ion implantation energy differs from the previous fabrication process. The arsenic ions were implanted with a dose of 5×10^{14} cm^{-2} and an energy of 10 keV. The activation was carried out by RTA at 950 ℃ for 30 s in N_2 atmosphere.

- A lift-off process was performed to deposit a stack of metals (200 nm Al) on the contact pads.
- In this process, we use annealing (400 ℃, 10 min) in rapid thermal processing (RTP) oven with N_2 and H_2 forming gases to form the ohmic contacts.

Afterwards, the wafer was cut and the samples were bonded for the measurements.

4.4 Si NW FET Biosensor Fabricated by T-NIL with Micrometer Channels

4.4.1 Chip Design

In this design, Si NW FET biosensors were designed and mainly based on 12 nanowire arrays without common source. The design is different from the case of backgate device, the chip size was 5×5 mm^2.

In order to avoid incomplete imprint resist transferring during the T-NIL, some sacrifice structures were added on the designed patterns, as shown in Figure 4.15 (left). In the previous measurements with the backgate devices, we find that, if one Si NW FET has leakage current, the whole chips cannot work well anymore. Therefore in this design, we developed the 12 arrays of Si NW sensors without common source. Every nanowire of the chip can work separately.

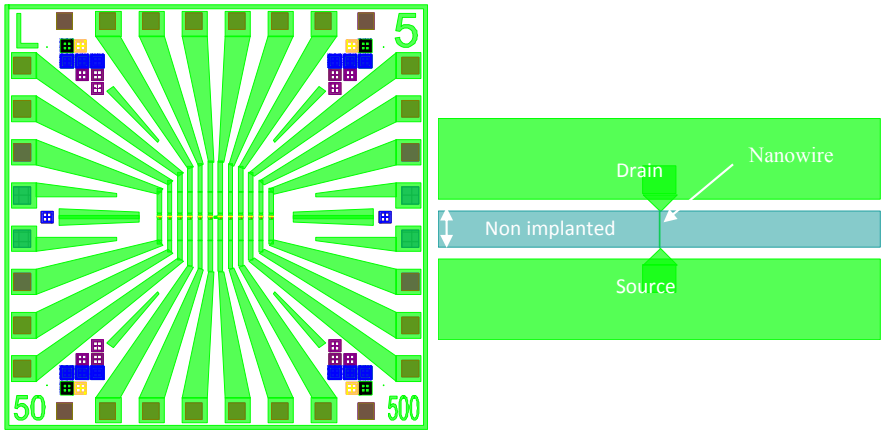


Figure 4.15 Layout (left) of the 12 × 2 Si NW sensor array with 24 drain and one common source and two backgate electrodes. The nanowire area (right) between source and drain contact line.

There are five kinds of devices in this design as shown in Table 4.7(a) and (b), one of them have same width of 250 nm, the length changes from 2 μm to 22 μm or 100 nm width and length change from 16 μm to 21 μm. Another kind of design is the set of structures with the same length of 4 μm, 5 μm and 20 μm, but the width changes from 50 nm to 500 nm.

The source and drain contact lines were highly implanted with arsenic and boron ions except the nanowire region where the doping level of the nanowires was as in the original SOI wafer one (Figure 4.15 (right)).

The contact lines and nanowires were fabricated using T-NIL, for a more detailed description refer to Appendix B.3.

Table 4.7 (a) The designed chips.

Chips Number	Name	Length L/μm												W/nm
5	L=2-22, W=250	2	3	4	6	8	10	12	14	16	18	20	22	250
5	L=16-21,W=100	16	17	18	19	20	21	21	20	19	18	17	16	100

Table 4.7 (b) The designed chips.

Chips Number	Name	Width W/nm												L/μm
5	L=4, W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	4
4	L=5,W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	5

5	L=20,W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	20

4.4.2 Chip Processing

The fabrication of this devices is the same as the backgated devices, only some of the steps are different:

The ion implantation processes for both P type and N type device are show in table 4.7, the activation of BF_2 was carried out by rapid thermal annealing (RTA) at 1000 °C for 5 seconds in N_2 atmosphere and activation of was carried out by RTA at 950 °C for 30 in N_2 atmosphere, respectively.

Table 4.7 Ion implantation

Ion	Ion implantation (B)	Ion implantation (As)
Energy	7 Kev, 7 degree, 1 x 10^{15} cm^{-2}	20 Kev, 7 degree, 1 x 10^{15} cm^{-2}
Activation	Activation of BF_2 was carried out by RTA at 1000 °C for 5 sec in N_2 atmosphere.	Activation was carried out by RTA at 950 °C for 30 sec in N_2 atmosphere.

Instead of 100 nm PECVD SiO_2 layer, SU8 was used as passivation layer against electrolyte solutions.

Afterwards, the wafer was cut and the samples were bonded for the measurement.

4.5 Si NW FET Biosensor with Submicrometer Channels Fabricated by EBL

4.5.1 Chip Design

In this design, we want to fabricate biosensor with short nanowires. We used EBL instead of T-NIL, which is a cost efficient technology, but it takes long time to make the mold and tune a lot of work parameters during the T-NIL.

The design is the same as the backgate FETs design in Chapter 4.3, except the omitting of sacrifice structure which was previously used to easy transferring the resist. The Si NW chips were mainly based on 12 × 2 arrays of Si NW sensors. The chip size was 3 × 3 mm^2 shown in Figure 4.16 (left). The chip included quite long contact lines for 24 individual drains and a common source contact to the nanowires. The contact lines and nanowires were fabricated using EBL, while the metal contacts were fabricated by a lift-off process at the end of the chip fabrication.

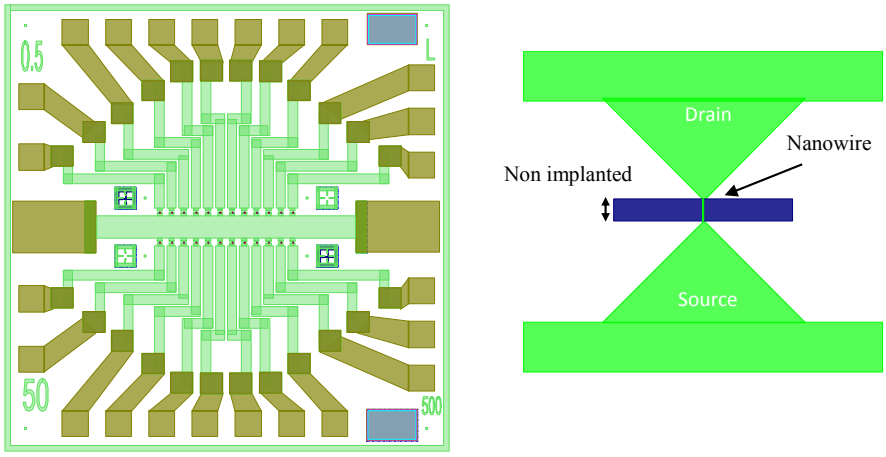


Figure 4.16 Layout (left) of the 12 × 2 Si NW sensor array with 24 drain and one common source and two backgate electrodes. The nanowire area (right) between source and drain contact line.

There are five kinds of devices in this design as shown in Table 4.8 (a) and (b), one of them have the same channel width of 50 nm and 100 nm, the length changes from 0.1 µm to 12 µm. Another kinds of design have the same length of 500 nm and 1 µm, but the width changes from 50 nm to 500 nm.

The source and drain contact lines were highly implanted with Arsenic ions except the nanowire region where the doping level of the nanowires was at the original SOI wafer doping level (Figure 4.16 (right)). For a more detailed description refer to Appendix B.4.

Table 4.8 (a) The designed chips.

Chips Number	Name	Length L/µm												W/nm
16	L=0.1-12, W=50	0.1	0.2	0.4	0.6	0.8	1	2	4	6	8	10	12	50
16	L=0.1-12, W=100	0.1	0.2	0.4	0.6	0.8	1	2	4	6	8	10	12	100
8	L=0.1-0.4, W=50	0.1	0.1	0.1	0.1	0.2	0.2	0.2	0.2	0.4	0.4	0.4	0.4	50

Table 4.8 (b) The designed chips.

Chips Number	Name	Width W/nm												L/µm
8	L=0.5, W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	0.5

8	L=1, W=50-500	50	100	150	200	250	500	500	250	200	150	100	50	1

4.5.2 Chip Processing

The fabrication of these devices is the same as the devices in Chapter 4.3, only some of the steps are different:

- The contact lines and nanowires were fabricated using EBL instead of T-NIL, the contact lines were written by coarse pattern parameter and the nanowires were written with using the fine pattern parameters and the small steps as shown in Table 4.9.

Table 4.9 The e-beam writing parameters with proximity effect correction used during the fabrication of the devices.

E-beam parameter	Dose($\mu C/cm^2$)	E-beam current (nA)	Beam step size (nm)
Conducting line (Coarse pattern dose)	300	150	50
Nanowire (Fine pattern dose)	300	0.2	2

- The ion implantation energy is different as the last fabrication process. The arsenic and boron ions were implanted with a dose of 5×10^{14} cm^{-2} with an energy of 20 keV and with a dose of 1×10^{15} cm^{-2} with an energy of 7 keV, respectively.

Afterwards, the wafer was cut and the samples were bonded for the measurement.

As it will be shown below, Si NW structures fabricated by the methods described are appropriate for future biosensing applications. To validate this according to the quality and transport properties of Si NW FETs, we perform measurements with different geometries of the channel and show good scalability. Results of electrical measurements show advanced properties of the fabricated structures with respect to sensitivity, reproducibility and reliability.

5. Performance and Scalability of Si NW FETs with Different Channel Lengths

Si NWs are the object of increased attention because along with nanoscaling they provide a number of new features in electronic transport [79]. In addition, their operating conditions differ significantly from those of conventional large-area MOSFET structures due to novel possibilities of controlling the current characteristics using dielectric engineering [80] and fine coupling effects tuned by applied gate voltages [81, 82]. Novel test structures fabricated on the basis of Si NWs are the ultimate building blocks for future nanoelectronics [83] and biological sensor applications [84]. These structures have to be stable in operation. However, a great many factors influence their reliability and stability, particularly the fabrication technology of NW-based structures.

The fabrication technologies of Si NWs can be divided into two categories: “bottom-up” and “top-down”. The bottom-up approach [85] relies on the Si NWs grown by CVD. The top-down approach [86] is more compatible with standard CMOS processes, and usually involves EBL and dry etching technologies. Top-down methods are currently attracting growing interest due to their unique advantages, such as high controllability, good reproducibility, and compatibility with state-of-the-art CMOS processing. These factors are very important for the fabrication of biosensors. However, almost all of the top-down processes use the RIE technique, which results in imperfections at the edges of nanostructures with a relatively low signal-to-noise ratio. T-NIL is a promising method for fabricating NW structures because of its low cost, high resolution, and high throughput. Anisotropic wet etching in TMAH produces a smooth surface and improved performance of the structures [23]. At the same time, it has been shown that a large stress may appear in top-down fabricated Si NWs [87]. Several reasons have been suggested for this stress, such as thermo mechanical stress, surface layers, and the deformation stress of dies. The oxidation process may also result in strain formation [88]. Strains in oxidized sample NWs were studied by analyzing X-ray diffraction curves [89]. The strains were found to be negative at the bottom surface and positive at the top surface of NWs, changing with depth in a concave way. In addition, the degradation processes in nanochannel FETs are greater than the negligible degradation in conventional MOSFETs [90]. The *I-V* characteristics of Si FETs show degradation due to Joule heating of the structures [91]. In high electric fields, hot carriers may generate interface traps, resulting in degradation of the FET threshold voltage [92]. It has already been demonstrated that the performance of Si NW structures is also determined by the microstructure of ohmic contacts to NWs [93].

However, despite progress in the technology and the ability to fabricate nanosize structures with identical geometry, structures of a similar size show rather large scattering in their electrical characteristics. This is primarily caused by traps and imperfections, by the utilization of very thin dielectric layers, and captures by these defect charges, which lead to a shift in the threshold voltage and change the transistor characteristics over time as these traps are charged. The values of voltages applied to the transistor also affect the processes in the

channel and the exchange processes with the traps. Noise spectroscopy is one of the most powerful methods for studying device performance and the reliability of structures with nanoscale dimensions, which is directly related to the type and number of traps in the structures. In this respect, the data obtained from noise spectra allows us to analyze the performance of the structure, to identify the main traps determining transport properties, and to predict the stability and reliability of the structures. Thus, noise properties directly reflect the performance of fabrication technology.

In this chapter, we describe the top-down method which we used to fabricate high-performance Si NW FET structures for biosensor applications applying cost-efficient T-NIL in combination with anisotropic wet etching in TMAH. We investigated the electrical properties of Si NW FET structures with different lengths. This enabled us to analyze the device transport properties that are presented below.

5.1 Experimental Details

We designed and fabricated Si NW structures with a width of 250 nm and different lengths (L = 2 µm, 3 µm, 4 µm, 6 µm, 8 µm, 10 µm, 12 µm, 14 µm, 16 µm, 18 µm, 20 µm and 22 µm) to investigate the effect of nanostructure scalability on device performance. The SOI wafers were purchased from SOITEC, France. The thicknesses of the buried oxide (BOX) and of the top Si layer (Si<100>, boron-doped 14-22 Ω cm) were 145 nm and 70 nm, respectively. The detailed design and the fabrication processes can be found in Chapter 4.2 and Appendix B.1.

The conductivity of the samples was modified by applying a voltage to the substrate used as the gate electrode. To tune the characteristics of the FETs, they were exposed to small doses of gamma irradiation using a standard isotope ^{60}Co source with a flux of 1 Gy/s and an energy of 1.2 MeV, using an accumulated dose of 10^4 Gy.

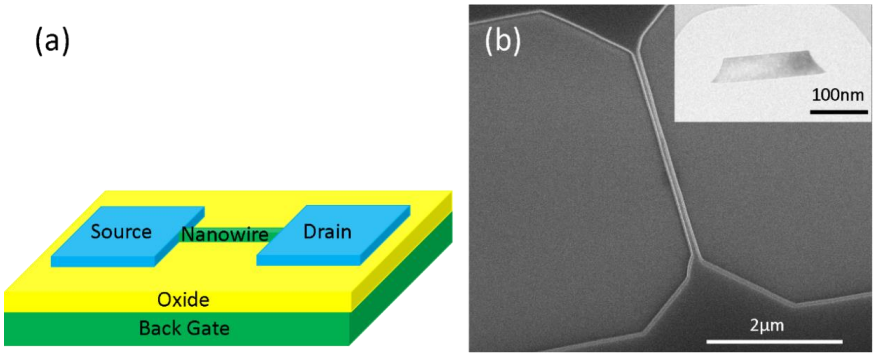


Figure 5.1 (a) Schematic of a Si NW FET showing a NW with source and drain regions on the surface of a SiO_2/Si substrate. Inset: high-resolution transmission electron micrograph of cross-section of a Si NW with a width of 250 nm. The scale bar is 100 nm. (b) Scanning electron micrograph of a fabricated Si NW. Inset: enlarged TEM image of the NW with a width of 250 nm.

Figure 5.1 (a) shows a schematic of a Si NW FET with source and drain regions on the surface of a SiO_2/Si substrate. While Figure 5.1 (b) shows a SEM image of a Si NW-FET device, the inset in Figure 5.1 (b) shows a high-resolution transmission electron micrograph (TEM) of a Si NW with a width of 250 nm.

The electrical properties of the back-gated nanowire FETs were studied using *I-V* characteristics and low-frequency noise spectra measurements at room temperature. A low-noise measurement setup was developed in-house based on an amplifier with a low level of intrinsic input-related thermal noise of 2×10^{-18} V^2Hz^{-1} This enabled the peculiarities of the noise spectra to be studied in the frequency range from 1 Hz to 100 kHz, and the characteristic parameters of the structures to be extracted as a function of channel length.

5.2 Transport Properties of Si NW FETs with Different Lengths

5.2.1 Current-voltage Characteristics of Fabricated Si NW FETs

The *I-V* characteristics for one of the Si NW devices with a length of 2 µm and width of 250 nm are shown in Figure 5.2. The drain-source current I_{DS} versus drain-source voltage V_{DS} characteristics were measured at various back gate voltages V_{BG} (Figure 5.2 (a)). These output characteristics demonstrate that the drain-source current increases with positive drain-source voltage and can be effectively controlled by the gate voltage. The transfer characteristics of the Si NW device are shown in Figure 5.2 (b). For a given V_{DS}, the I_{DS} shows a considerable increase with positive gate voltages V_{BG}. This indicates an n-channel behavior of the transistor. A characteristic feature of these samples is a slow drift (decrease) in the drain current when drain-source voltage is applied over a long time of about 2 hours. The transfer characteristics registered in the short-time regime (5 min after voltage application) and after a longer period (2 hours) differ. In the second case, the measurements were performed after the establishment of the quasi-steady state. The value of the threshold voltage V_{Th} was determined as -1.26 V.

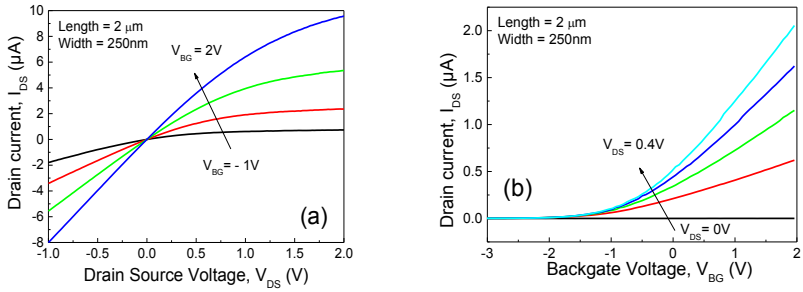


Figure 5.2 (a) Typical output I_{DS}-V_{DS} characteristics of the Si NW FET with a width of 250 nm and length of 2 µm measured at different backgate voltages V_{BG} in the range from -1 V to 2 V with a step of 1 V. The arrow indicates the increasing value of the back-gate voltage. (b) Transfer characteristics of the FET, measured at increasing drain voltage V_{DS} in the range from 0 V to 0.4 V with a step of 0.1 V.

The transfer characteristics of Si NW FETs of different lengths are shown in Figure 5.3. The measurements were performed at a low drain voltage (V_{DS} = 100 mV). The transfer characteristics demonstrate good scalability depending on the nanowire length for different NW FETs. The transition from the linear I_{DS} (V_{BG}) to a sublinear dependence at V_{BG} > 1.5 V was typical for all samples. It should be noted that the above-described dependences were measured at an applied drain-source voltage after 2 - 3 hours, i.e. when the stable state was reached in the structures. Measurement results in the high-speed regime (measuring time: a few seconds) demonstrated no transition to a sublinear dependence. These data demonstrate that at V_{DS} = 100 mV and at gate voltages larger than 1.5 V, slow traps are charged slowly in the dielectric layer by negative charges, which leads to a shift in the threshold voltage and results in a reduced concentration of free electrons in the channel.

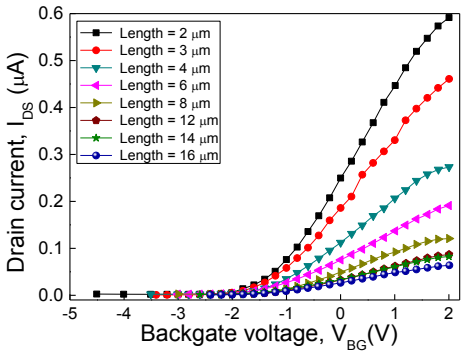


Figure 5.3 Transfer characteristics measured at V_{DS} = 100 mV for Si NW sample with width W = 250 nm and different lengths in the range of 2 µm to 16 µm.

Figure 5.4 (a) shows the total resistance as a function of channel length, obtained at different gate overdrive voltages, V_{BG} - V_{Th}. The extracted contact resistances of the samples using the transmission line model (TLM) are shown in Figure 5.4 (b). We can clearly see that the contact resistance decreases as the gate bias increases. This decrease in contact resistance can be explained by taking into account the small voltage drop over the contact regions due to increased charge carrier concentration in the conducting channel at high gate biases. The width of the Schottky barrier on the drain side is narrowed by the accumulation of electrons at higher gate biases. This reduces the tunneling distance and increases the tunneling current through the narrower Schottky barrier from the channel region to the drain electrode. As a result, the parasitic contact resistance decreases.

There was almost no registered change in the threshold voltage, which was estimated to be -1.26 V as a function of the length of the sample down to L = 4 µm. A sharp decrease was observed for samples with lengths of L = 3 µm and L = 2 µm. This effect in samples with short channels can be explained by contact phenomena at the interface between the ion implantation feedline region doped by As atoms and the sides of the nanowire channel of unintentionally doped silicon.

The results demonstrate that the contact resistance is lower than the total resistance, and we can neglect the contact effect of the drain and source on the channel conductivity for samples with lengths above 4 µm.

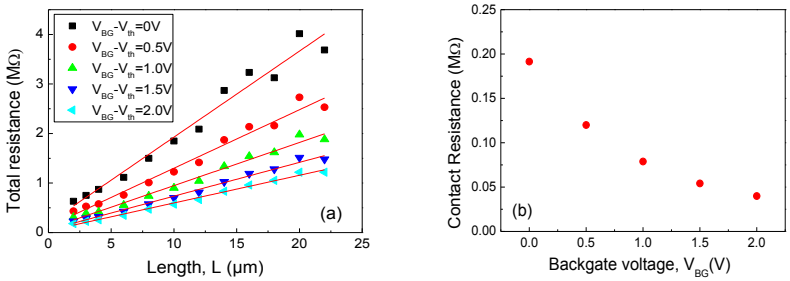


Figure 5.4 (a) Total resistance of Si NW FET devices as a function of channel length, measured at low drain voltage V_{DS} = 100 mV and different overdrive gate voltages, $V_{BG} - V_{Th}$: 0 V, 0.5 V, 1.0 V 1.5 V, 2 V. (b) Contact resistance extracted from TLM structures of different lengths. These data demonstrate nonlinear dependence on gate overdrive voltage.

For MOSFET devices, field-effect mobility can be extracted from transfer characteristics using the following relation [94]:

$$\mu_{eff} = \frac{L^2 g_m}{C_{ox} V_{DS}} \tag{5.1}$$

where L is the gate length, g_m is the transconductance and C_{ox} is the NW to back-gate capacitance. It follows from data shown in Figure 5.5 that our NW devices exhibit a much higher mobility than the values usually reported in the literature [26]. This is due to a higher degree of confinement and the high quality of the NW fabrication process, which produces a smooth surface.

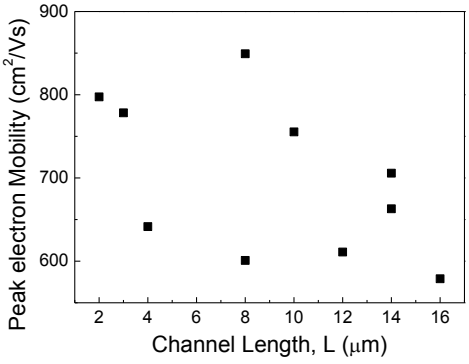


Figure 5.5 Electron mobility (μ_{eff}) extracted for Si NW FET devices with different channel lengths.

5.2.2 Noise Spectra of Fabricated Si NW FETs

Noise measurements of NW FET samples of different lengths showed that the spectra mostly demonstrated $1/f$ behavior. A study of noise behavior as a function of gate voltage showed that the main source of noise is the exchange process between the carriers and traps in the dielectric layer. This process can be described by the McWhorter model [95]. The input-referred noise spectral density is usually used to analyze the noise properties of the structures. Such equivalent input gate voltage noise was determined as a function of the gate in accordance with the following expression:

$$S_U = \frac{S_I}{g_m^2} \tag{5.2}$$

where S_I is the current channel noise, and g_m is the transistor transconductance, which can be determined from the slope of the transfer characteristic of the transistor using the following expression:

$$g_m = \frac{dI_{DS}}{dV_G}|_{V_{DS}=const} \tag{5.3}$$

The transconductance dependences on gate voltage are shown in Figure 5.6:

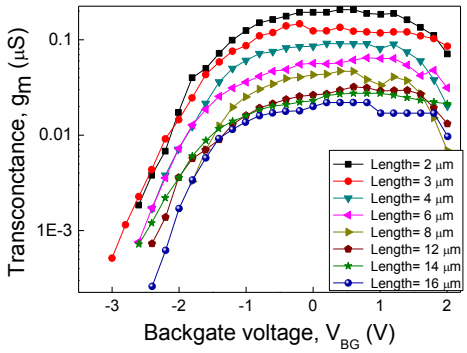


Figure 5.6 Transconductance of Si NW FETs with a width of 250 nm and different lengths as a function of gate voltage V_{BG}, measured at low drain voltage V_{DS} = 100 mV.

In some cases, well-resolved Lorentzian noise components were registered in the spectra above the flicker noise. These components were observed in the spectra of short samples at high gate voltages. Typical families of spectra measured for samples with a length of 2 μm are shown in Figure 5.7**.**

In the noise spectra measured for samples of short lengths (L = 2-4 μm), Lorentzian noise components were also resolved (Figure 5.8). These components correspond to random RTS noise, measured as a function of time.

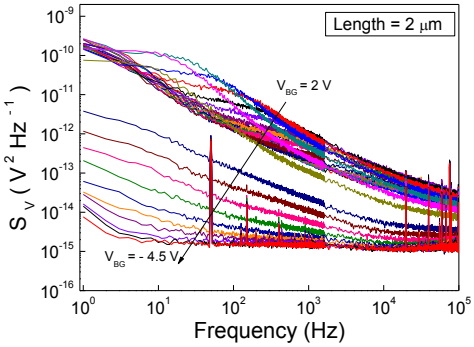


Figure 5.7 Measured noise spectral density for a Si NW FET sample of length L = 2 µm at gate voltages from 2 V to -2.6 V.

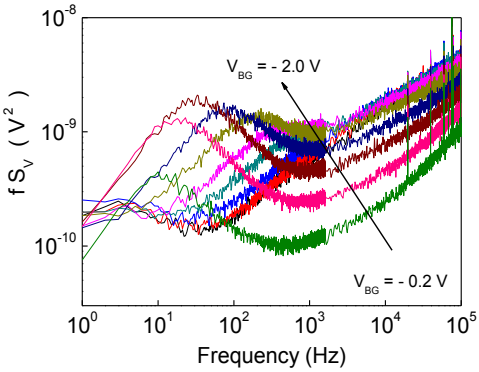


Figure 5.8 Normalized noise spectral density for the Si NW FET sample with length L = 2 µm measured at different gate voltages in the range from 0.2 V to 2.0 V with a step of 0.2 V.

5.2.3 Analysis of Flicker-noise Component

The noise level was set to 1/*f* noise at the frequency *f* = 1 Hz. Dependence of this parameter on the gate voltage is shown in Figure 5.9: 1/*f* noise at *f* = 1 Hz.

These dependences are typical of MOSFET structures. A weak dependence was observed in the accumulation regime at high voltages and a sharp decrease in the subthreshold regime. Peaks were observed at times at voltages close to the threshold V_{Th}. Further analysis was performed using equivalent gate voltage noise (Figure 5.10).

The dependence of 1/*f* noise at the frequency of *f* = 1 Hz was plotted as a function of the gate voltage and used to obtain the input-related noise spectral density S_U as a function of V_{BG}, as shown in Figure 5.10.

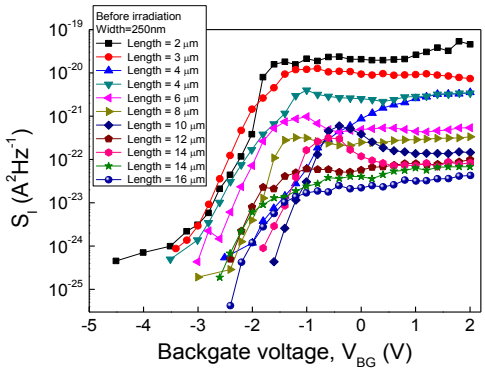


Figure 5.9 Measured noise spectral density of flicker noise 1/*f* at *f* = 1 Hz as a function of gate voltage V_{BG}.

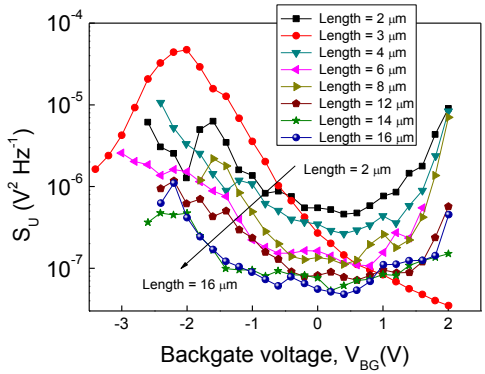


Figure 5.10 The input-referred noise spectral density S_U as a function of gate voltage V_{BG}, obtained for Si NW FETs of different lengths.

These dependences are typical of MOSFET structures. A weak dependence was observed in the accumulation regime at high voltages as was a sharp decrease in the subthreshold regime. With the exception of a sample of length L = 3 µm, S_U behavior was similar for all samples: a relative independence of gate voltage between -1 V < V_{BG} < 1.5 V and an increase in the V_{BG} > 1.5 V and V_{BG} < -1 V. In the first case, the increase can be explained by taking into account the different behavior of the static and dynamic g_m in this voltage range (as discussed above).

In the second case involving large negative gate voltages, the growth of the S_U at V_{BG} < -1 V can be explained as follows.

At negative values of V_{BG}, the channel is depleted, and when these negative values increase further, an inversion layer forms near the bottom of the interface layer. This layer screens the channel from the influence of gate voltage (and from voltage fluctuations), which leads to a slower change in the drain current with gate voltage in this area (Figure 5.10). Therefore, the

noise in the subthreshold regime is no longer determined by the states in the bottom interface, but rather by the states in the upper interface between the passivation dielectric layer and the channel. In this case, the charge fluctuations in the dielectric layer transform in the channel with a different slope defined by the upper dielectric layer. For this voltage range, the values of S_U, which are calculated using the measured values of g_m using the back gate, are overestimated.

In addition, the presence of inversion layer in the channel can result in a number of processes related to the restructuring of the channel. The first process involves the formation of two p-n junctions connected in series: the forward-biased source/inverse channel and the reverse-biased junction formed by the inverted channel drain. This leads to a current associated with recombination (forward-biased junction) and generation (reverse-biased junction). Generation-recombination processes of this type are reflected in the spectra in addition to the $1/f$ noise of the Lorentzian noise component, particularly in the samples of short length (Figure 5.6). The current increase at large negative V_{BG} is also associated with this phenomenon. The second process is caused by the presence of a dielectric interface on the top channel, which can lead to the "floating base" effect [96], which also results in additional noise with a characteristic frequency determined by internal capacitances.

At moderate voltages independent of back-gate voltage V_{BG}, the plateau (Figure 5.10) corresponds to the flicker noise associated with a bottom dielectric layer. It should be noted that the noise level in this region differs (by about one order of magnitude) for samples of different lengths. However, this difference is much smaller than the difference of three orders of magnitude in the S_I values (Figure 5.9). The data in Figure 5.9 show the $S_I \sim L^{-3}$ dependence, confirming the applicability of the McWhorter model [95] with:

$$S_U(f) = \frac{kT\lambda q^2 N_{ot}(E_F)}{fWLC_{ox}^2} \propto \frac{1}{WL} \tag{5.4}$$

where N_{ot} (E_F) is the trap density in the dielectric layer, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate insulator capacitance per unit area, ε_{ox} is the permittivity of the dielectric layer, t_{ox} is the oxide thickness, $\lambda = \sqrt{\hbar^2/2m_z^*\varphi_b} = 10^{-8}$ is the tunneling distance, T is the temperature, k is the Boltzmann constant, q is the electron charge, φ_b is the potential barrier between the channel and the gate dielectric, $\hbar$ is the reduced Plank's constant, m_z^* is an effective mass of the carriers, and W is the width of the sample.

The experimental results obtained (Figure 5.11) demonstrate that S_U is reciprocally dependent on length $1/L$ at $V_{BG} = 0$.

Using Equation (5.4), we can determine the volume trap density of active sites in the lower dielectric layer, substituting $\varepsilon_{ox} = 3.9\varepsilon_0$ and $t_{ox} = 145$ nm, $S_U = 10^{-7}$ V^{2}Hz^{-1}, $L = 10$ µm, $W = 0.25$ µm: N_{ot} is about 5×10^{17} cm^{-3}eV^{-1}. This value is not as high as that obtained from bulk Si material [97].

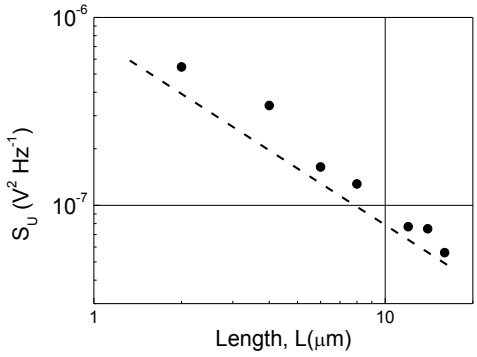


Figure 5.11 The input-referred noise spectral density S_U as a function of L at V_{BG} = 0. Dashed line shows *1/L* dependence.

5.2.4 Estimation of the Hooge Parameter

In order to compare the noise level of our devices with noise values reported in the literature, we estimated the Hooge parameters using Equation (5.5) [98]:

$$S_I = \frac{\alpha_H I_D^2}{fN} \tag{5.5}$$

where N is the number of carriers and α_H is Hooge's constant, which is used to quantitatively assess and compare the noise performance of our devices.

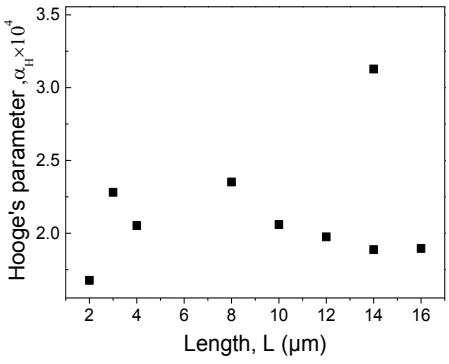


Figure 5.12 Hooge parameters for Si NW FET structures of different lengths.

The total number of carriers, N, in the working point with the maximum of the transconductance using the following equation

$$N = \frac{I_D L^2}{q V_{DS} \mu} \tag{5.6}$$

The average Hooge parameter (Figure 5.12) for the devices was below 2×10^{-4} for Si NW fabricated using developed nanoimprint technology. This value is much lower than the values reported in the literature for silicon nanostructures [99], demonstrating the improved technology and performance of Si NW FETs.

5.2.5 Gamma Radiation Treatment

Typical output characteristics of Si NW FETs measured before and after gamma radiation treatment with a dose of 10^4 Gy are shown in Figure 5.13**.** The measurements were performed in a linear regime at V_{DS} = 100 mV for samples with a uniform width of 250 nm and different lengths.

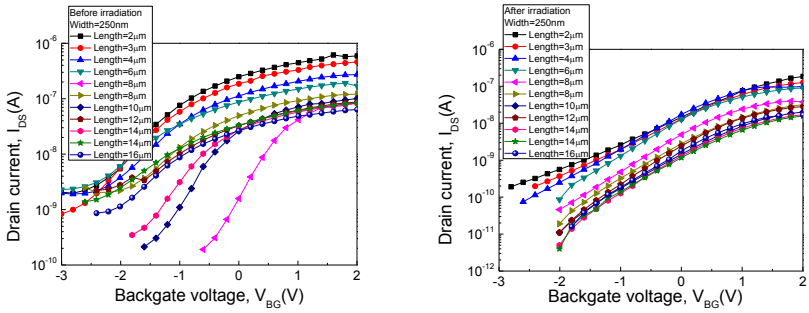


Figure 5.13 Output characteristics of Si NW FETs (a) before and (b) after gamma radiation treatment measured at V_{DS} = 100 mV for samples of different lengths in the range from 2 μm to 16 μm.

It should be noted that subthreshold current is strongly reduced after the treatment by an average of about one order of magnitude. Before gamma irradiation, V_{Th} was -1.26 V (except for samples of length 8 μm and 12 μm). After irradiation, the threshold voltage shifted to a positive value of 0.295 V. In addition, the scattering of characteristics reduced after treatment, while the reducibility of electric parameters improved.

Further analysis of NW FET transport properties before and after gamma radiation treatment was performed using the results of the noise study. Figure 5.13 shows the normalized measured 1/*f* noise obtained at a frequency of 1 Hz. It should be emphasized that there are specific differences in the noise characteristics: in the irradiated samples at a subthreshold voltage, noise is relatively weakly dependent on the gate voltage, and the non-irradiated characteristics demonstrate a sharp peak at V_{BG} - V_{Th} = -0.5 V, followed by a sharp decrease at large negative biases.

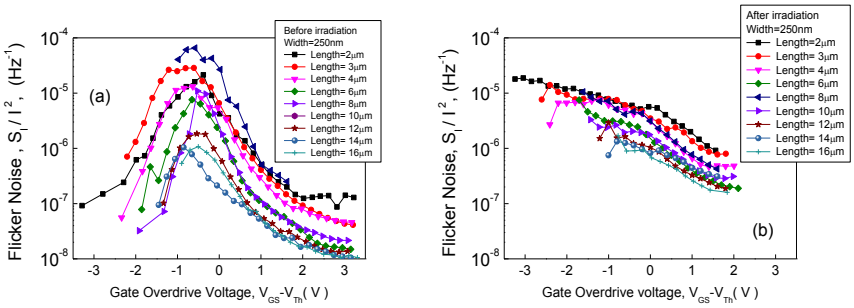


Figure 5.14 1/*f* noise at a frequency of 1 Hz measured (a) before and (b) after gamma radiation treatment as a function of overdrive gate voltage V_{BG} - V_{Th}.

The spectra measured for short-length samples also reveal Lorentzian-type noise components in addition to the 1/*f* noise component (Figure 5.15). An analysis of fluctuation behavior as a function of time showed that the Lorentzian noise components correspond to the RTS-type noise, i.e. the noise is associated with fluctuations related to a single center. Measurement results for the RTS noise component for short-length samples demonstrated that there is a significant contribution of this kind of noise before irradiation (Figure 5.15), but that after exposure, the level of the RTS noise component significantly reduces, and the characteristic frequency decreases from 1.6 kHz to 40 Hz. At the same time, the slope drain-gate characteristics reduce slightly with back-gate voltages, as shown above. This can be explained by the shift of the conductive channel to the upper interface, and the reduced influence of the back-gate voltage on the channel. In this case, the electron density at the lower interface decreases as does the probability of the GR process, manifested in the form of RTS noise, leading to a shift in the spectrum of RTS to low frequencies. Since the bottom interface no longer exhibits high current density, the noise level decreases.

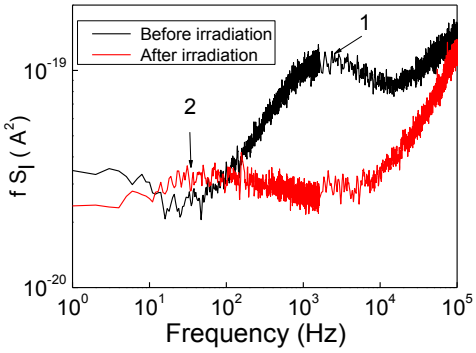


Figure 5.15 Normalized current-noise spectral density measured in the strong inversion for a Si NW FET sample with a width W = 250 nm and length L = 2 µm (1) before and (2) after gamma radiation treatment.

The shift in the maximum frequency of Lorentzian RTS after irradiation (Figure 5.15, red curve) can be explained by changes in the charge state of the center from the positively charged (attracting) state to neutral, or from neutral to a negatively charged (repulsive) state. This results in a decrease in carrier concentration for exchange processes between the channel and dielectric layer. In turn, this causes a decrease in the probability of the carrier being captured and, consequently, an increase in the time constant, which determines the position of the maximum frequency in the noise spectrum.

The reduction in the amplitude of RTS noise in the irradiated sample can be explained as follows. RTS noise modulates, i.e. charge fluctuations of a single center modulate the conductivity of the channel with high density. These regions arise because of the inhomogeneity of the semiconductor characteristics in the channel area.

Irradiation removes mechanical stress in the contact region, which also reduces $1/f$ noise and RTS noise levels. The fact that the RTS noise was only observed in short-channel devices confirms the near-contact origin of the observed RTS fluctuations.

In the subthreshold regime, the slope of the drain current-gate voltage characteristic reduces twice, which represents a reduced influence on the conduction channel of the bottom gate bias. Such changes in the conditions at the lower interface influence the subthreshold current, which after exposure practically disappears. The shift in the threshold voltage to positive values of gate voltage indicates an increase in negative charge at the interface. At the same time, it is known that γ-irradiation leads to an increase in the concentration of positive charge due to the difference in nobilities of electrons and holes. This contradiction may be explained by percolation transport before gamma radiation treatment due to non-uniform potential redistribution along the SOI wafer. Radiation stimulated a more uniform redistribution of the potential. This resulted in a change from a negative to a positive threshold voltage and reduced scattering in device characteristics.

5.3 Summary

In this chapter, high quality of nanowire FETs fabricated by TMAH wet etching and T-NIL technology were described. This fabrication method is a promising low-cost and CMOS-compatible method. The results of electrical measurements show that the contact resistance is smaller than the total resistance and that we can neglect the contact effect from the drain and source for samples with lengths greater than 4 μm. The characteristic time constants corresponding to the capture of the carriers were determined by analyzing RTS noise spectra components. Trap density, estimated from flicker noise, was found to be about 5 x 1017 cm-3, which is of the order of magnitude of good-quality bulk silicon material. The improved technology and TMAH chemical etching produced samples with a high mobility and low noise level. Such devices can be employed as chemical or biological sensors with a higher sensitivity to the object being tested due to a high level of uniformity and performance. The data, an analysis of the RTS noise component, registered for samples of short length before gamma

treatment, was reduced after this treatment, reflect the improvement brought out by irradiation via stress relaxation in the contact regions.

As it will be shown in the next chapter, such an RTS will be studied from the point of view of channel conductivity modulation by a single trap in the gate oxide. Such phenomena can be used as new principle to develope ultra sensitive devices.

6. Modulation Phenomena in Si NW FETs Characterized Using Noise Spectroscopy

FET based on Si NWs are an important step in the miniaturization of CMOS devices to obtain state-of-the art devices for information technology. They are the ultimate building blocks for modern electronic devices and biosensors [100-102]. Utilized for electronics, Si NW FETs allow high-frequency operation and lower power consumption. As biosensors, NWs provide higher sensitivity and spatial resolution compared with conventional planar FETs due to their higher surface to volume ratio [103]. By considering the transport in Si NWs, one may see that the current in the Si NW FET is determined by the much lower quantity of carriers than in conventional CMOS FETs due to the small device size. Obviously, this results in higher fluctuations of the conductivity and transport modulation of the NWs. One of the objectives of the biological and bioelectronic utilization of Si NWs as sensors is detection of the interaction of a single molecule with the Si NW surface [15]. To be able to distinguish such a response under the level of native fluctuations of a Si NW, a comprehensive investigation of transport in Si NWs has to be performed. The analysis of the fluctuations in the Si NW FETs combined with *I-V* characterization contains all the information about performance and transport phenomena in the device. This information is of extreme importance for device development and further improvement of the fabrication technology.

Noise spectroscopy makes it possible to analyze the performance and structure of the samples under study by investigating the fluctuation phenomena. The method itself is a powerful tool for characterizing the dynamic properties of the investigated structure, and hence, for the extraction of information about the origin of noise in the sample. Noise spectroscopy can be used for the analysis of the device quality, transport properties and improvement of the technology, which is one of the main directions for the development of advanced NW FETs and miniaturization of the elementary basis of CMOSs.

The excess noise spectrum of silicon transistors usually contains GR noise components related to traps with definite energy and a flicker noise component, known as $1/f$ noise, as a result of the trap contribution from contact regions and traps related to gate dielectric or mobility fluctuations [58, 97, 104]. The $1/f$ noise of MOSFETs is usually analyzed in the frame of the McWhorter model, which describes flicker noise by charge carrier trapping/detrapping from the conducting channel to the traps located inside the gate dielectric layer [105].

The Influence of γ-irradiation on the FETs allows the parameters of the devices to be changed in a controlled way [106, 107], which may be used for studies and even to improve their characteristics [108]. In addition, the method can be used to slowly change the parameters of the sample without exerting a strong influence on the device. Thus characterization of the transport in Si NW transistors can be unambiguously performed using γ-irradiation of the samples with small doses. This allows the material parameters to be changed precisely, because the dose of the absorbed radiation can be controlled by accumulation with time.

Here I present the results of comprehensive transport studies of p-type Si NW FETs. The devices are characterized by noise spectroscopy, which enables us to study subtle transport effects. Using noise spectroscopy, a strong modulation of the channel conductivity is revealed even under the influence of a single trap. Analysis of the $1/f$ component of the excess noise allowed the volume trap density in the thin dielectric layer to be estimated for the samples measured. In these terms, the investigated Si NW FETs demonstrate high quality and improved device performance. The Lorentzian components of the noise spectra are registered, and their behavior allows the trapping/detrapping processes of the gate dielectric traps to be characterized. The parameters of the single trap, which generates the RTS noise, in the gate dielectric layer were determined. Investigation of samples after treatment by gamma irradiation with a dose of 10^4 Gy confirms the influence of trap charges on conductivity in the channel of NW FETs.

6.1 Experimental Details

The structures under investigation are p-type NW-FETs with a cross-section of ≈ 42 x 42 nm^2 fabricated at Forschungszentrum Jülich using a top-down approach on the basis of 50 nm SOI wafer (N_A = 1 x 10^{15} cm^{-3}, buried oxide thickness of 145 nm). An N-type polysilicon gate electrode was deposited on the 5 nm thermally grown SiO_2 gate oxide layer, which covered each of the NWs. Source/drain contacts to NWs were formed by ion implantation of boron with an energy of 10 keV and a dose of 1 x 10^{15} cm^{-2} followed by rapid thermal annealing. Thus, the samples represent transistors with inversion *p*-channel. The polysilicon covers the NW channel to form a tri-gate (Figure 6.1) in the middle part of the NW channel. The tri-gate configuration offers improved gate control over the channel compared to planar geometry. The transistors are in the off-state at zero biases on the front gate and substrate, which plays the role of back gate. The current through the samples can be tuned either by front gate or by back gate voltages.

Noise spectra of NW-FET devices with lengths of 1.5 µm and 3 µm were investigated under different regimes defined by drain- source biases, V_{DS}; front-gate voltages, V_{FG}; and back-gate voltages, V_{BG}. The schematic of the noise measurement setup is shown in Figure 3.5. The bias voltages (drain-source and gates) are applied using a battery to avoid circuit fluctuations. Variable resistors allow the values of the applied voltages to be changed. Spectra were acquired in the frequency range from 1 Hz to 100 kHz. The samples were irradiated using a ^{60}Co source of gamma rays with a dose of 10^4 Gy and energy of 1.2 MeV.

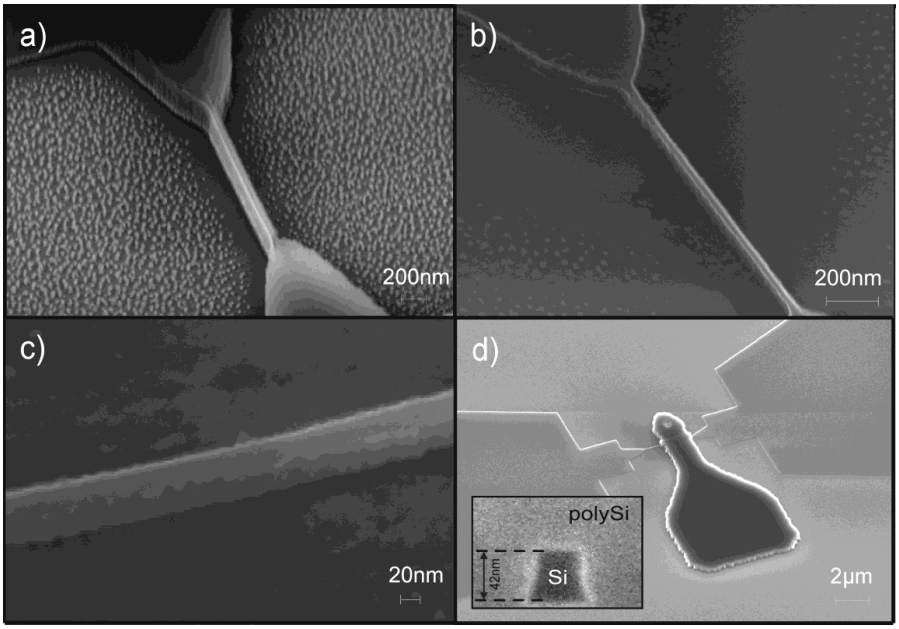


Figure 6.1 (a-c) SEM image of Si NW device. (d) SEM image of Si NW devices with polysilicon gate. Inset in (d): focused ion beam cut of the wire under study.

6.2 Results and Discussion

6.2.1 Electric Properties before and after Gamma Irradiation

The output curves of the investigated samples are shown in Figure 6.2. Their behavior is characteristic for metal-oxide semiconductor devices. It should be noted, that all noise spectra were measured at low drain bias (around 100 mV), which provides a linear mode of operation of the transistors in almost the entire range of gate voltages (Figure 6.2).

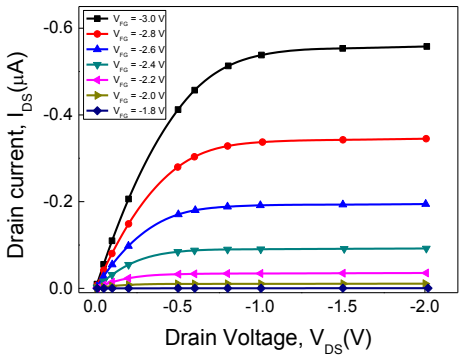


Figure 6.2 Typical output characteristics of one of the NW samples under study. Backgate voltage: V_{BG} = 0.

Transfer *I-V* characteristics for the 1.5 µm and 3 µm samples are shown in Figure 6.3.

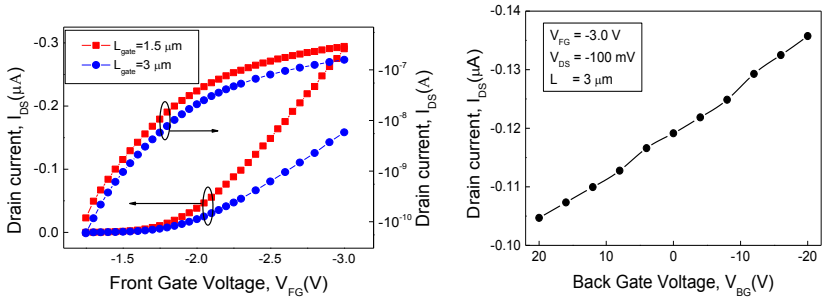


Figure 6.3 Transfer curves measured (a) for samples with different lengths (1.5 µm and 3 µm) at drain bias of -100 mV, zero back gate voltage as a function of front gate voltage. (b) for sample of the 3 µm length versus back-gate voltage at drain bias of -100 mV and front-gate voltage of -3 V.

The curves reflect the reproducible scaling with decreasing length of the samples. Typical maximum transconductance values g_{m_max} for 3 µm and 1.5 µm samples are 1.3 x 10^{-7} and 2.7 x 10^{-7} A/V, respectively. Samples have almost the same threshold voltage (V_{Th} ~ -1.95V). The current in the samples shows much weaker dependence on back-gate voltage (Figure 6.3 (b)) compared with front-gate voltage. This is due to the fact that the buried oxide is significantly thicker than the front-gate oxide layer. It is known that traps in dielectric layers can be affected by using low doses of gamma radiation. Therefore the characteristics of the samples were investigated both before as well as after gamma radiation treatment. The experimental transfer curves $I_{DS} = f(V_G)$ of the non-irradiated and irradiated samples at zero substrate bias and different back gate voltages are shown in Figure 6.4.

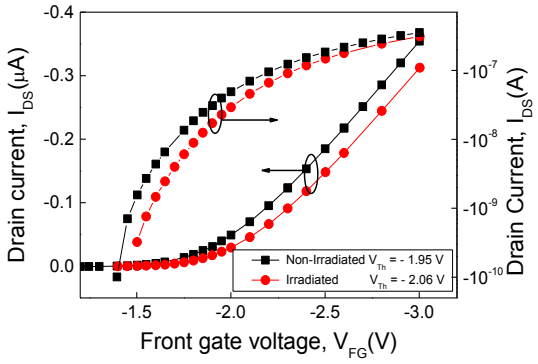


Figure 6.4 Typical transfer *I-V* curves measured for 1.5 µm samples at drain bias of -100 mV and zero back gate voltage before and after irradiation treatment.

It can be seen that after irradiation treatment the threshold voltage increases and the change in the slope of the transconductance curves is negligibly small. The numerical values of the parameters extracted from Figure 6.4 data are summarized in Table 6.1.

Table 6.1 Characteristics of the samples before and after irradiation treatment.

Sample gate length	1.5 µm		3 µm	
Value	V_{th} (V)	g_{m_max} (S)	V_{th} (V)	g_{m_max} (S)
Before irradiation	-1.95	3.4×10^{-7}	-1.95	1.8×10^{-7}
After irradiation	-2.06	3.3×10^{-7}	-2.06	1.8×10^{-7}

As can be seen from Table 6.1 and Figure 6.4, the irradiation treatment influences the threshold voltage of the samples, but does not affect the g_{m_max}. The data demonstrate that the irradiation changes the surface charge of the Si NW without affecting the average scattering times of the impurities inside the channel. The data will be used below.

6.2.2 1/*f* Noise Spectroscopy

Typical noise spectra of one of the samples measured at several front gate voltages are shown in Figure 6.5 (a). The spectra contain two noise components: 1/*f* and Lorentzian shaped.

Using the measurements of noise spectra and *I-V* characteristics, the volume trap density of the gate dielectric layer can be estimated [58, 109]. This density of traps reflects the quality of the gate dielectric and can be compared for different dielectric layers to optimize the dielectric compositions for miniaturization of the final device. During the process of device downscaling (i.e. from micron width to the submicron scale), at some size even the response of the single traps can be registered. In this case, excess noise contains not only the flicker noise component but also a number of separate Lorentzian components [53, 110]. At a certain level of downscaling the device size approaches a limit, at which one or several traps in the dielectric modulate the current. In this case, the signal as a function of time in the device demonstrates the random telegraph signal (RTS) [53, 104, 111-114] noise behavior. Analysis of the RTS spectra and time trace allows us to investigate the parameters of the individual traps of nanoscale devices. Individual molecules can play the role of a single trap on the surface of the device, which in this case may be used as the molecule sensor [15, 115].

Equivalent input spectral density is used to calculate volume trap density. 1/*f* noise current spectral density (S_I) component can be used to calculate the equivalent input spectral density, *Su*, [29]:

$$S_U = \frac{S_I}{g_m^2} \tag{6.1}$$

where g_m – is the derivative of the drain current on gate voltage derived from Figure 6.3 (a). Typical S_u dependence is shown in Figure 6.5 (b) for samples of different lengths. The equivalent input power spectral density demonstrates a weak dependence on gate voltage, which indicates that the McWhorter model is applicable for estimating the gate oxide volume trap density [58, 97, 116]. The density, N_t, can be calculated in the frame of the McWhorter model as follows:

$$N_t = \frac{S_I \alpha_t C_{ox}^2 WLf}{g_m^2 q^2 kT} \tag{6.2}$$

where α_t is the inverse tunneling depth, C_{ox} is the specific gate oxide capacitance, W is the channel width, L is the channel length, f is the frequency, q is the electron charge, k is the Boltzmann constant and T is the temperature. In our case, T is about 293 K. Here, α_t can be estimated using:

$$\alpha_t = \sqrt{\frac{2m_h^* \varphi_b}{\hbar^2}} \tag{6.3}$$

where φ_b is the potential barrier between channel and gate dielectric, m_h^* is an effective hole mass and $\hbar$ is the reduced Planck's constant. The specific capacity of the gate oxide can be obtained as:

$$C_{ox} = \frac{\varepsilon \varepsilon_0}{t_{ox}} \tag{6.4}$$

where ε is the dielectric permittivity of the silicon oxide layer, ε_0 is dielectric permittivity of vacuum, t_{ox} is the gate oxide thickness, which in our case is equal to 5 nm.

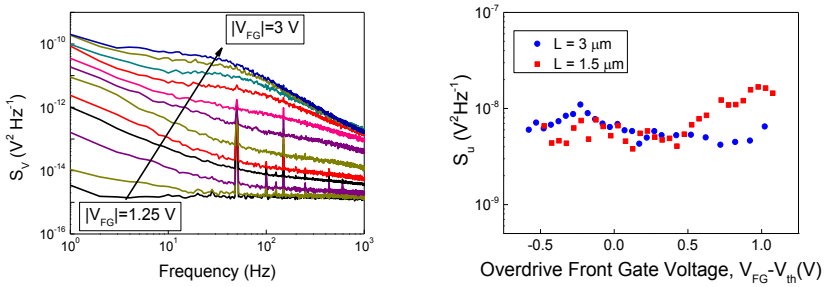


Figure 6.5 (a) Noise spectra measured for 3 μm sample at different front gate voltages at drain-source bias of 100mV. (b) Equivalent input voltage spectral density for two samples with different lengths estimated for the difference of overdrive gates, V_{FG}-V_{th}.

Using Equation (6.2) we estimated the value of the volume trap density for all measured samples. The obtained values are within the range from 1 x 10^{17} cm^{-3} eV^{-1} to 5 x 10^{17} cm^{-3} eV^{-1}. It should be noted that these values are about one order of magnitude lower than those obtained for submicron CMOS devices [97]. By multiplying the obtained values of N_t by the oxide thickness t_{ox}, the surface trap densities were obtained for our samples. They are expected to be in the range between 5 x 10^{8} cm^{-2} eV^{-1} and 2.5 x 10^{9} cm^{-2} eV^{-1} .The densities are much lower than estimated for the thin film dielectric layers of MOS transistors [117].

6.2.3 Lorentzian Components and Single Trap

Investigation of the time traces of the noise signal measured on the samples under study showed that a random telegraph signal (RTS) noise is the origin of the low-frequency Lorentzian components in noise spectra. The RTS noise component is a characteristic feature of low-scale samples taking into account that 1/*f* noise from the point of view of the McWhorter theory can be represented by superposition of Lorentzian components in the case of a large-sized sample. In the case of large-area samples, the multiple dielectric traps, equally randomly distributed by energy and depths, result in a 1/*f* spectrum of the excess noise. At some characteristic size (tenths of nanometers) of the transistor channel, the noise of the channel can be determined mainly by the single trap in the gate dielectric with energy close to the Fermi level [53, 110]. In this case, the noise may even be observed from the individual oxide trap in the form of RTS that dominates the flicker noise. It should be noted that the above-mentioned individual oxide trap is of the same nature as those traps that are responsible for 1/*f* noise in the frame of the McWhorter model [53]. The spectra of both components, Lorentzian and 1/*f* noise, can be analyzed separately [53, 118].

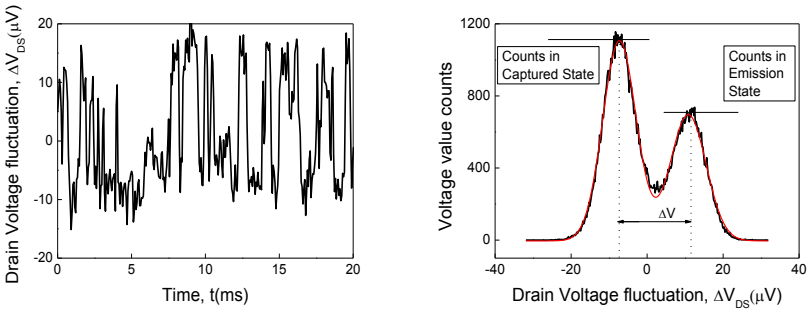


Figure 6.6 (a) Random telegraph signal noise time trace measured for 3µm sample at V_{DS} = -100 mV, V_{FG} = -3 V. (b) Histogram for the voltage values for the time trace obtained from (a).

The flicker noise separated into single Lorentzian noise components represents a remarkable opportunity to investigate the single trap properties and predict the properties of samples with a large number of traps in the gate dielectric. Analysis of the RTS time trace allows the capture and emission time constants to be estimated as well as the RTS amplitude for a single trap. Using these data, the capture cross-section of a trap and its position in the gate oxide layer can be calculated. The data obtained can be used to optimize nanoscale Si NW FETs. The

RTS noise was registered for the samples with different lengths for a wide range of applied gate voltages. Figure 6.6 (a) shows the typical time trace of measured RTS noise. We used a statistical method to calculate the capture and emission time on the basis of these data [119]. If the voltage time trace contains two well-resolved levels, we can construct a histogram of voltage values (shown in Figure 6.6 (b)).

The histogram of the RTS trace separates into two clearly resolved Gaussian peaks. The ratio of peak heights corresponds to the relation between capture and emission times (τ_c and τ_e), because the height of each peak is related to the time that the system spends in each state. The distance between the peaks equals the RTS amplitude ΔV, which can be recalculated to the ΔI – difference in current between captured and emission states. The time constant τ of the Lorentzian spectra that corresponds to the RTS noise can be expressed as [53]:

$$\tau = \frac{\tau_c \tau_e}{\tau_c + \tau_e} \tag{6.5}$$

Using the τ_c/τ_e relation obtained from the histogram and the value of τ obtained from the spectra, the values of τ_c and τ_e can be obtained.

Histograms of RTS time traces obtained for different front-gate and back-gate voltages are shown in Figure 6.7 (a) and Figure 6.7 (b). Data of Figure 6.7 (a) (related to the Lorentzian component of the spectra shown in Figure 6.5 (a) demonstrate that the values of capture and emission times depend on the front gate voltage. In contrast, RTS traces of Figure 6.7 (b) express negligible dependence on the back gate voltage. The fact demonstrates that the trap which results for the RTS modulation of the sample conductivity is located in the top gate dielectric.

The calculated values of τ_c and τ_e are plotted versus the overdrive gate voltage in Figure 6.8 (a). Obviously, dependencies $\tau_c(V_G - V_{th})$ and $\tau_e(V_G - V_{th})$ contain much more information about generation-recombination processes than the resulting time constant of a corresponding Lorentzian spectra component.

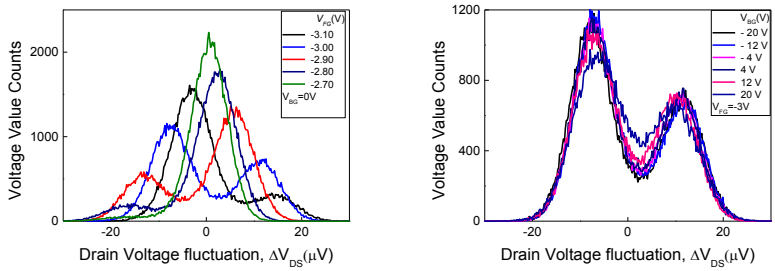


Figure 6.7 Histogram of the RTS noise time trace for 3 μm sample obtained at different front-gate voltages (a) and at different back-gate voltages (b).

6.2.4 Characteristic Time Constants and Position of Single Trap

RTS spectroscopy provides advantages for the characterization of trap parameters such as depth, position along the channel and capture cross-section [53]. In order to find the position of the trap in the gate oxide we investigated the dependence of the τ_c/τ_e relation on front-gate voltage. The depth of the trap in the gate oxide is calculated as follows [111, 120]:

$$x_t = -t_{ox}\frac{kT}{q}\frac{d(ln(\frac{\tau_c}{\tau_e}))}{dV_{FG}} \tag{6.6}$$

As discussed above, the relation between capture and emission times can be obtained directly from the histograms of the RTS time trace. This relation is shown in Figure 6.8 (b), obtained for different front gate voltages. The data demonstrate that the logarithm of the τ_c/τ_e depends linearly on the front gate voltage and, hence, Equation (6.6) can be used to find the trap depth. Using the t_{ox} as 5 nm for the samples under study and the linear minimum least squares fit of the data shown in Figure 6.8 (b), we estimate the trap depth x_t to be in the range from 1.65 nm to 1.85 nm for all measured samples.

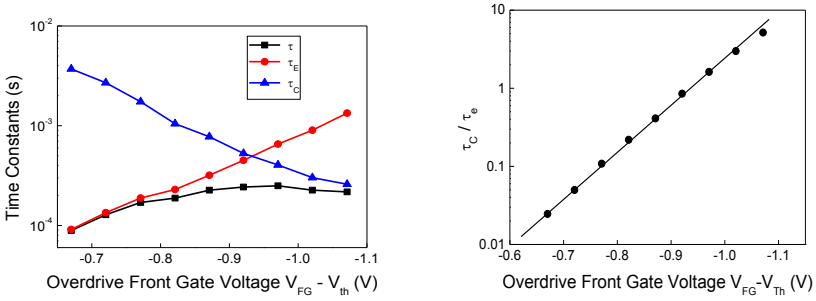


Figure 6.8 (a) Time constant of the Lorentzian noise component obtained from Figure 6.5, calculated emission and capture times as a function of overdrive gate. (b) Calculated relation between capture and emission time plotted versus front-gate voltage.

The dependence of the time constants of the RTS noise on the drain-source bias contains information about the position of the active trap along the channel length. Therefore, to study the behavior of the active dielectric traps, we investigated the noise of the samples in the nonlinear regime at a fixed front-gate voltage of V_{FG} = - 3.0 V and different channel biases V_{DS} = -0.01..-2.0 V (Figure 6.9). In addition, measurements were also made for the reverse polarity of the drain-source bias. Increasing the drain voltage V_{DS} shifts the channel to the nonlinear regime followed by saturation (Figure 6.2). With increasing bias voltage on the transistor channel, the gate dielectric voltage, which forms an inverse channel, decreases from $\Phi_s = V_{FG}$ to $\Phi_s = V_{FG} - V_{DS}$. From Figure 6.9, it follows that the time constant determined by the RTS noise component is reduced with increasing drain voltage. As we have already discussed above, increasing the drain voltage decreases the Φ_s near the drain to the value of $V_{FG} - V_{DS}$ and hence it decreases the concentration of carriers in the inversion channel near the drain

electrode. These facts indicate that the Lorentzian component of the noise spectra is mainly determined by the emission time constant τ_e. Indeed, a decrease of the concentration of free carriers in the inversion channel causes the increase of the probability of emission of free carriers from the centers located in the dielectric layer and, consequently, leads to a decrease in the emission time constant from 2.5 x 10^{-4} to 5.0 x 10^{-5} s.

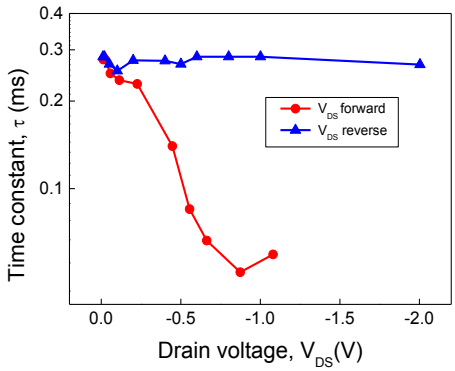


Figure 6.9 Time constant of the Lorentzian component of the noise spectra of the sample plotted versus drain voltage at V_{FG} = - 3.0 V, V_{BG} = 0. Red circles correspond to the G-R processes at forward polarity of channel bias; blue triangles correspond to the GR-process at reverse polarity.

In the case of a reverse bias of the Si NW transistor, we can see from Figure 6.9 that the emission time constant does not depend on the drain voltage. This fact demonstrates that there are no changes in the concentration of free carriers in the vicinity of the corresponding capture center. Such behavior of the time constant with changes of the drain voltage is only possible if the center is located at a site where the influence of the applied drain voltage is negligibly small (where the gate dielectric voltage Φ_s is constant and does not depend on V_{DS}). Thus we conclude that the dielectric trap, which generates the RTS noise in the investigated sample, is located in the gate dielectric layer close to only one of the ohmic contacts of the Si NW transistor.

6.2.5 Modulation Effects Related to Single Carrier Process

The amplitude of RTS fluctuations is an important value, which reflects the impact of a single surface charge on the channel conductivity [121, 122]. Dependence of the amplitude ΔI of the RTS fluctuations is shown in Figure 6.10. The amplitude is almost constant in the shown range of front-gate voltages and equals 0.20 ± 0.01 nA.

This can be explained as follows. Capture of a free carrier on the fixed trap in the dielectric excludes it from the conductivity. The charged state of the trap results in shielding of part of the channel. At constant voltage V_{DS} applied to the channel, the exclusion of fixed charge in the regime of strong inversion leads to a decrease in the current ΔI. At the same time, the current amplitude does not change. This fact demonstrates that also the mobility remains

constant in this range of gate voltages. If we assume that only one carrier is excluded from the channel during the capture and that shielding effects are negligible, then we can write

$$\Delta I = I(N+1) - I(N) = \frac{1}{V} e\mu_{eff} ES = \frac{1}{V} e\mu_{eff} \frac{V_{DS}}{L} S = \frac{e\mu_{eff} V_{DS}}{L^2} \qquad (6.7)$$

where *N* is the quantity of carriers, *L* is the length of the channel, *S* is the area of the channel cross-section, *V* is the volume of the device, which equals *LS*, μ_{eff} is the mobility of the holes, V_{DS} is the drain-source bias. Using Equation (6.7), the mobility of holes for the sample can be estimated. The calculated value exceeds 1000 cm^2/Vs, which is obviously too high for the hole mobility in silicon devices. Thus we can conclude that capture of the free carrier on the traps causes a modulating effect on current in the NW channel. Capture of one hole considerably modulates current in the channel (which is equivalent to the exclusion of more than one hole from the transport in the transistor channel). This fact demonstrates the possibility of single molecule detection with increased sensitivity using the modulation effect of the channel conductivity in Si NW FET.

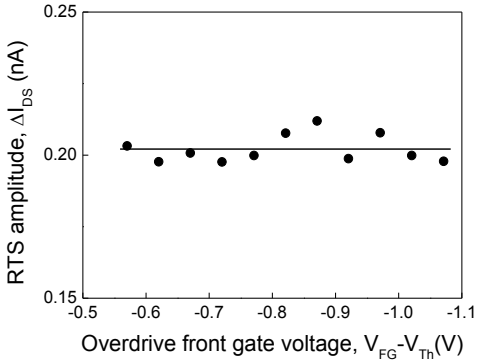


Figure 6.10 The RTS noise amplitude dependence on the overdrive front-gate voltage. V_{BG} = 0, V_{DS} = -100 mV.

6.2.6 Single Trap Properties and Parameters

The obtained RTS parameters allow us to estimate a capture cross-section of the dielectric trap. According to the Shockley-Reed-Hall theory, capture and emission times can be calculated as follows [53]:

$$\tau_c = \frac{1}{\sigma n v_{th}} \text{ and } \tau_e = \frac{1}{\sigma n_1 v_{th}} \qquad (6.8)$$

where σ is the capture cross-section of the trap, *n* is the concentration of the carriers in the channel, n_1 is the the concentration of the carriers in the channel when the Fermi level coincides with the energy of the trap, v_{th} is the thermal speed of the carriers. The thermal speed is equal to

$$\bar{v} = \sqrt{\frac{3kT}{m^*}} \tag{6.9}$$

where m^* is the effective mass of the carriers. Taking into account that T = 293 K, the effective mass of the hole is equal to 0.56 of the electron mass, m^* = 5.10 x 10^{-31} kg, the thermal speed is obtained as 1.55 x 10^5 m/s. Then the value of the capture cross-section can be estimated using Equation (6.8). It should be noted that *n* is considered to be a constant value and the capture cross-section includes tunneling and thermo-activation processes, as will be discussed below. Thus the obtained value will be a rough approximation. However, under conditions of high currents this approximation can be accepted [53]. The concentration and the carrier mobility were estimated using the transfer curve [20] of the NW transistor with the following relations:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \frac{W}{L}\mu_{eff}C_{ox}V_{DS} \tag{6.10}$$

$$I = nevS = ne\mu_{eff}ES \approx ne\mu_{eff}\frac{V_{DS}}{L} \tag{6.11}$$

where μ_{eff} is the carrier mobility, S = *W* x *H*, is the cross-section of the channel, *H* is the height of the channel, *E* is the electric field, which can be estimated in the linear region using the drain-source bias voltage and the length of the sample.

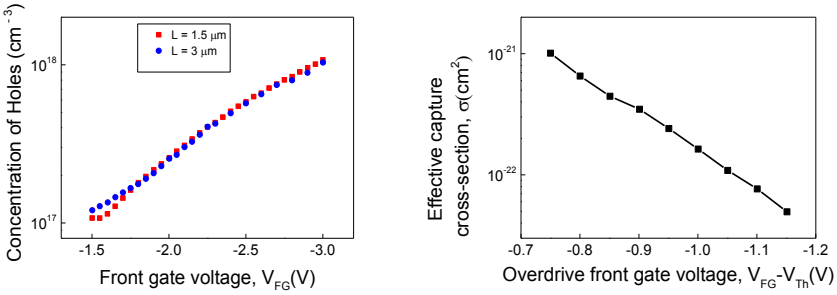


Figure 6.11 (a) Calculated concentration of holes as a function of applied gate voltages. (b) Dependence of the calculated effective capture cross-section of the trap on the overdrive gate.

The characteristics can be obtained:

$$\mu_{eff} = \frac{g_m L}{W C_t V_{DS}} \tag{6.12}$$

$$n = \frac{I_{DS} C_{ox}}{q g_m H} \tag{6.13}$$

Using Equation (6.12) and data from Figure 6.2, we estimated hole mobility for NW samples to be in the range from 120 to 150 $cm^2 V^{-1} s^{-1}$. The calculated values of hole concentrations are shown in Figure 6.11 (a). It should be noted that the concentrations are the same for the samples with different lengths manufactured on the same wafer.

The fact that the trap is located in the gate dielectric means that the carriers have to overcome the barrier to be captured on the gate oxide trap. Therefore a new multiplier: $e^{\frac{\Delta E}{kT}}$ should be added to Equation (6.8), which is sequence of the Shockley-Reed-Hall theory [53, 123]:

$$\tau_C = \frac{e^{\frac{\Delta E}{kT}}}{\sigma n v_{th}} \tag{6.14}$$

where ΔE represents the energy needed to overcome the barrier from the channel of the device to the trap through the oxide layer. At low concentrations of the carriers in the channel, this energy depends on the gate voltage, but at high drain currents, where the product of capture time τ_c and the drain current I_{DS} becomes independent of drain voltage the value of the trap capture cross-section can be estimated using the Shockley-Reed-Hall theory, particularly without the exponential term [112, 122]. For some of the investigated samples, the condition discussed above can be fulfilled at high front-gate voltages. Thus using Equation (6.8), values of τ_c and calculated concentrations, we estimate the capture cross-section of the single trap located in the gate dielectric to be not higher than $2x10^{-21}$ cm^{-2}, which corresponds to the repulsive trap [53, 113, 123]. Strong dependence of the capture cross-section on the front-gate voltage (see Figure 6.11 (b)) can be explained by a shift of the centroid of the inversion layer to the Si/SiO_2 interface with increasing surface potential, Φ_s [53, 56, 113, 123]. Therefore, dependence of the capture cross- section σ on gate voltage (Figure 6.6 (b)) reflects the change of ΔE as a function of V_{FG}. This fact additionally proves that the trap is located in the gate dielectric.

6.2.7 Tuning of Carrier Exchange by γ-irradiation

Parameters of the traps can be tuned by γ-irradiation [124]. Therefore, utilizingγ-irradiation treatment allowed us to obtain knowledge about the nature of traps as well as about the mechanisms of influence of such a treatment on the performance of Si NW devices. A shift of threshold voltage (Figure 6.4) behavior is demonstrated and discussed above. Changing of the dielectric trap parameters is monitored utilizing noise spectroscopy (Figure 6.12).

Comparing the noise values at different frequencies, it may be concluded that the characteristic frequencies of the Lorentzian components shift to the lower frequency after irradiation. The noise of the above-mentioned traps shows similar behavior to the RTS noise. The shift reflects the fact that the capture probability (inversely proportional to time constant τ) of traps in the dielectric layer becomes lower near the threshold as well as in strong

inversion regimes. As follows from Equation (6.14), the value of capture cross section of the trap has decreased, if we assume that the values of ΔE and n are constant. Moreover, the time constant changes by about two orders of magnitude, and the capture cross section σ also becomes lower by two orders of magnitude. Such behavior can be explained by the changing of a trap from neutral to repulsive (positively charged) [125]. This fact is additionally confirmed by the shift of the threshold voltage to an increased level corresponding to a more positive potential of Si/SiO_2 interface. Therefore irradiation leads to changes in the charge state of the dielectric traps, which shifts the threshold voltage and, on the other hand, impacts the conditions of the carrier exchange between traps and the conducting channel.

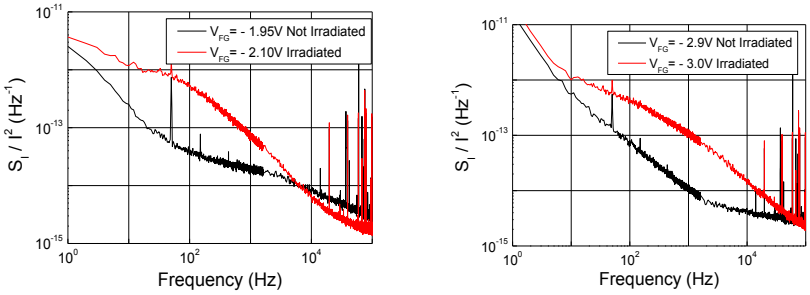


Figure 6.12 Normalized current noise spectral density of the Si NW FET measured before and after gamma irradiation near the threshold (V_{FG} - $V_{th} \approx 0$) and in the regime of strong inversion ($V_{FG} - V_{Th} \approx$ -1 V), reflecting the characteristic shift of the Lorentzian components.

6.3 Summary

Transport properties of p-type Si NW FETs (with a cross-section of ≈ 42 x 42 nm^2 fabricated at Forschungszentrum Jülich) utilizing noise spectroscopy are studied. The devices possess low excess noise level. The values of volume trap density obtained from the level of input voltage spectral density are much lower than those obtained for conventional CMOS devices. The devices with different channel lengths have almost the same input voltage spectral density indicating that the influence of contact effects on the performance of the investigated devices can be neglected. The nature of the changes in the defect structure of the Si NW samples under low doses of gamma radiation was analyzed. In particular, our measurements demonstrate that low doses of gamma irradiation result in a shift the threshold voltage, without any influence on the scattering times inside the channel and the mobility. Low doses of gamma irradiation change the charge state of the traps located in the gate dielectric, which confirms that the origin of noise is related to gate dielectric traps. Analysis of the registered RTS noise component reveals that a single trap is located near one of the ohmic contacts in the gate dielectric. Estimated parameters of the trap and its behavior demonstrate that even a single carrier process in the gate of the NW transistor considerably modulates current in the channel. These results are promising for advanced control of the channel transport in NW FETs, including the possibility of single molecule detection with increased sensitivity using the modulation effect of the channel conductivity in Si NW FET.

To understand the observed RTS Phenomena in more detail, we also analyze the influence of the Coulomb Blockade energy of the single trap on Si NW FET channel transport in the next chapter. A variable temperature study was undertaken to thoroughly investigate this phenomena. Later, the remarkable sensitivity of charge detection using capture times will be discussed in Chapter 10.

7. Coulomb Blockade Energy in Si NW FET

Nowadays Si NW FETs have attracted much interest not only being used as the building blocks of state-of-the-art transistors [126], but also it can be used as biosensors because of their ultrahigh surface-to-volume ratio [8, 23]. However, low frequency noise is becoming a serious issue for highly scaled dimensions. Capture and emission of charge carriers by interface traps is the source of either carrier number fluctuation or induced mobility fluctuation, resulting in the flicker noise (1/*f* noise). When such capture/emission processes are dominated by an individual trap, the current of the device switches between two levels, resulting in RTSs in time domain. Especially, in these small devices, the charging dynamics of individual traps become obvious [127, 128].

Shockley-Read-Hall (SRH) statistics is a general model applied to describe the emission and capture rates [129, 130]. However, experiments with submicron transistors show, that the capture kinetics of RTS in submicron FETs cannot be described accurately by this simple SRH model. Such a deviation can be explained by the consideration of the Coulomb Blockade energy [56, 123].

As in the last chapter, we have registered RTSs in short channel FETs and found the RTSs phenomena to be potentially useful for biosensing. It inspired us to fabricate sub micrometer channel devices using T-NIL in combination with standard CMOS technology. As we expected, RTSs were registered in the fabricated devices.

The devices are characterized by low frequency noise spectroscopy, which enables us to study the transport properties as well as capture dynamics of the RTS trap. The Lorentzian components of the noise spectra were registered and their behavior allows characterization the trapping/detrapping processes on the gate dielectric traps. The measured data are evaluated to extract the Coulomb Blockade energy and its functional dependencies on temperature and mobile carrier concentration in the MOSFET channel.

7.1 Experimental Details

T-NIL was used to transfer the micro and nano structure to SOI wafer (Soitec). The pattern was transferred through the active silicon layer using TMAH anisotropic wet etch (25% in H_2O at 90 °C). Source and drain regions were doped by As^+ ion implantation with energy of 10 keV and a dose of 1 x 10^{15} cm^{-2} followed by rapid thermal annealing. EBL was used to define HSQ resist as the mask. At last, a layer of 100 nm PECVD SiO_2 was used as the passivation layer. The devices were then metalized by Al evaporation and patterned by lift-off through the opened contact pad. The substrate was used as a back gate. The detailed design and the fabrication processes can be found in Chapter 4.3 and Appendix B.2. One of the Si NWs was shown in Figure 7.1.

The transfer characteristics were measured by a probe station, from which the subthreshold slopes and field-effect mobility was extracted. Noise measurements were performed under DC conditions using our noise setup. The devices were biased at a drain-source voltage of 0.1 V, and the gate voltages were chosen so that the devices were always operated in the linear region of the I_{DS} - V_{BG} (transfer) curve. The bias voltages (drain-source and gates) are applied using a battery to avoid circuit fluctuations. Variable resistors allow the values of the applied voltages to be changed. Spectra were acquired in the frequency range from 1 Hz to 100 kHz. The measurements were characterized in the temperature range from 200K to 280K.

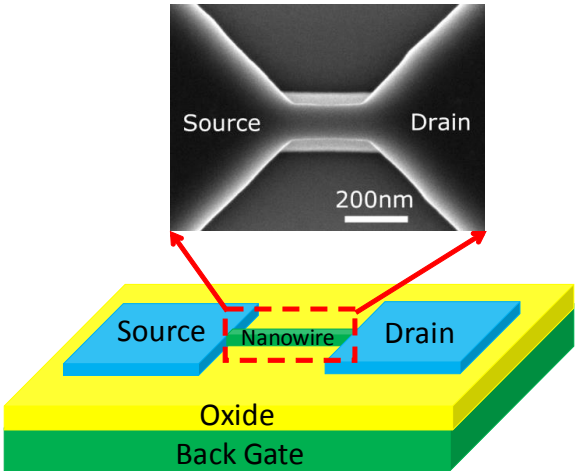


Figure 7.1 Schematic diagram and SEM image of Si NW FET.

7.2 Results and Discussion

7.2.1 Electrical Measurements of Fabricated Si NW FETs

In this work, Si NW FET with 500 x 500 nm^2 channel was characterized using probe station and low frequency noise spectra setup.

Figure 7.2 (a) shows a family of output characteristics: I_{DS} (V_{DS}) of the FETs. The data demonstrate that the linear region of the FETs can be registered in the range of drain-source voltages: $V_{DS} \approx$ -0.2 V - +0.2 V. Transfer characteristics of Si NW FETs and their noise spectra were measured in the linear regime, below drain source voltage V_{DS} = 100 mV.

Typical transfer characteristics of the NW FETs are shown in Figure 7.2 (b), the device exhibits a subthreshold slope of S = 200 mV/dec at room temperature and reveals a characteristic of short-channel effects as the scaling of the channel lengths and thick backgate oxide layer. Drain induced barrier lowering (DIBL) with a value of 760 mV/V was extracted from the transfer characteristics. In the case of the output characteristics, DIBL results in a finite slope in saturation of the Si NW FET instead of a constant saturation current as for long-channel devices.

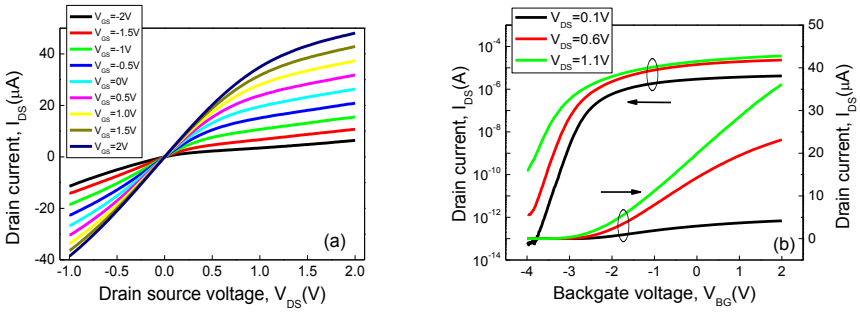


Figure 7.2 Output (a) and transfer (b) characteristics of Si NW FET sample with channel 500 × 500 nm².

7.2.2 Low-frequency Noise Spectra Measurements

Measured noise spectra of Si NW devices demonstrate mainly $1/f$ dependence. Such kind of the spectrum is typical for MOSFET structures. In a range of temperatures (T = 200-280 K), we observed two-level random telegraph signal (RTS) noise components, which enables us to study and to characterize a single center, located near the Si-SiO_2 interface in bottom dielectric layer of SOI wafer. Average capture time constant, τ_c, and emission time constant, τ_e, characterize generation-recombination processes at the single trap center of the bottom dielectric and these characteristic times were studied as a function of temperature. The corresponding dependencies are shown below (Figure 7.3).

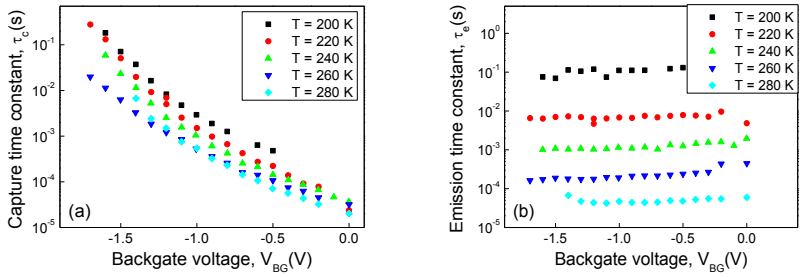


Figure 7.3 Dependence of the capture time constant τ_c (a) and emission time constant τ_e (b) on the gate voltage V_{BG}, measured at different temperatures, listed in the figure.

It should be emphasized, that the value of the capture time constant τ_c depends strongly on the V_{BG} and relatively weakly depends on temperature. At the same time the value of the time constant emission τ_e is almost independent of V_{BG} and is strongly dependent on temperature.

Figure 7.4 demonstrate the amplitude of RTS noise as a function of the gate voltage V_{BG} measured at different temperatures. It can be plotted in the coordinates $\Delta I_{DS}/I_{DS} = f(I_{DS})$ (Figure 7.5) and I_{DS} serve as a measure of the electron concentration at the interface between channel and the dielectric at a constant drain voltage of 0.1 V. As can be seen at low currents (I_{DS} < 1.3 μA), value of $\Delta I_{DS}/I_{DS}$ is mostly independent of the current, and then decreases monotonically.

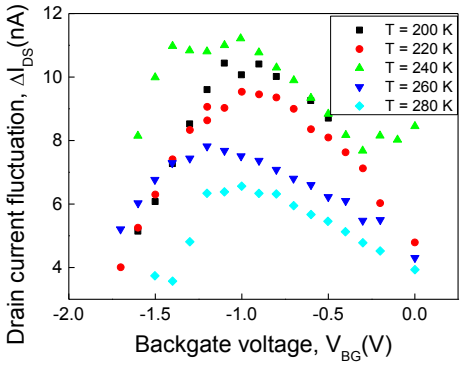


Figure 7.4 Dependence of the amplitude of RTS noise as a function of the gate voltage V_{BG} measured at different temperatures, listed in the figure.

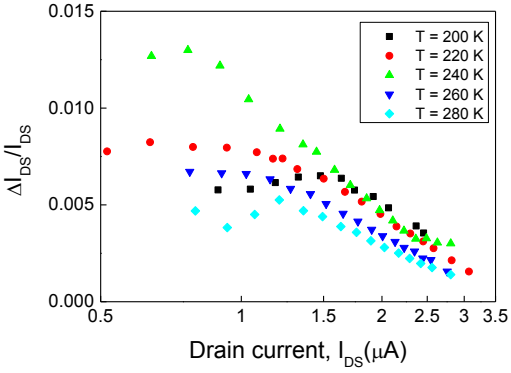


Figure 7.5 Dependence of the normalized amplitude of RTS noise as a function of the drain-source current I_{DS} measured at different temperatures, listed in the figure.

7.2.3 Analysis of Obtained Results

Analysis of the results dynamic characteristics of the active centers in semiconductors is usually performed in the frame of the Shockley-Read-Hall (SHR) model [129, 130], according to which:

$$\tau_c = \frac{1}{\sigma_n v_{th} n} \tag{7.1}$$

$$\tau_e = \frac{1}{\sigma_n v_{th} n_1} \tag{7.2}$$

Where σ_n is the capture cross section, v_{th} is the average thermal velocity, n is the concentration of electrons (in the case of electron capture) in the channel, n_1 is the statistical factor for the trap occupancy, when the Fermi level equals to the trap level.

According to Equation (7.1), at a certain temperature *T*, capture time τ_c is inversely proportional to the concentration of free electrons n. In our case, we can use the fact that this value determines the amount of current through the channel. If the mobility dependence on the gate voltage can be neglected, then the applicability of the model SHR can be checked by plotting $\tau_c = f(I_{DS})$. This dependence is shown in Figure 7.6. It should be emphasized that the current I_{DS} here is proportional to the concentration of free electrons at the interface.

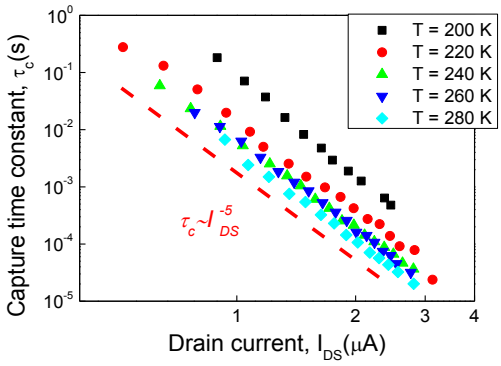


Figure 7.6 Dependence of the time constant of the capture τ_c as a function of the drain-source current I_{DS} measured at different temperatures. The dashed red line indicates a power law with exponent -5.

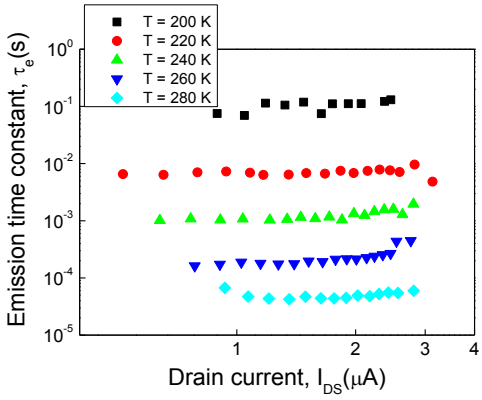


Figure 7.7 Dependence of the time constant of the emission τ_e as a function of the drain-source current I_{DS} measured at different temperatures.

Curves in Figure 7.6 demonstrate the exponential behavior. In the case of the model SHR, the slope of this dependence usually equals -1. It should be noted that in our case the dependence

is more strong: $\tau_c \sim I_{DS}^{-5}$. The reasons for this behavior are widely debated in the literature [53, 131-134]. Most acceptable model proposed in Ref. [56, 123, 135, 136].

Figure 7.7 shows the time constant of the emission τ_e as a function of the drain-source current $I_{DS.}$

The main difference of the exchange of electrons between a trap and an array of free carriers in the case of bulk semiconductors and in the case of MOSFET structures – the fact that in the latter case, the electron pass some distance from its location to the trap through the dielectric layer. This requires additional energy ΔE, which is associated with energy consumption in the process of charging of the capacity MOS structure. This additional energy is known in the literature as the Coulomb Blockade energy [137-141]. In this case, the time constants of the capture and emission of a neutral center can be expressed as follows [123]:

$$\frac{1}{\tau_c} = C_n N_C e^{-(E_C - E_F)/kT - \Delta E/kT} \tag{7.3}$$

$$\frac{1}{\tau_e} = C_n N_C e^{-E_b/kT} \tag{7.4}$$

where $C_n = \sigma_n v_{th}$ is the coefficient ratio of electron capture, N_C is the density of states at the bottom of the conduction band, E_C is the energy level of the conduction band, E_F is the Fermi level, $E_b = E_C - E_{T0}$ is the energy of the center, E_{T0} is the energy position of the center of the Coulomb energy.

The values of C_n and N_C provided in the case of thermodynamic equilibrium can be eliminated by taking the ratio of the left and right sides of Equation (7.3) and Equation (7.4):

$$\frac{\tau_e}{\tau_c} = e^{-(E_C - E_F - E_b + \Delta E)/kT} \tag{7.5}$$

In the case of SHR model, the ratio of the time constants depends only on the difference ($E_C - E_F - E_b = E_{T0} - E_F$). From Equation (7.5), we obtain the values of the Coulomb energy ΔE, first by determining the value of E_b using Equation (7.4) and by calculating the value $E_C - E_F$. However, these calculations are enough cumbersome, therefore I don't put the whole procedure here. The evaluation of chosen variables can be performed on the basis of expressions from Equation (7.3) - (7.5).

Above we have listed some values depending on the current in the channel in the assumption that the drain current is proportional to the concentration of electrons at the interface at all studied temperatures. This assumption, however, does not take into account three factors. The first one is the heterogeneity of inverse electron concentration and the second one is the temperature dependence of the mobility, the third one is the temperature dependence of the $C_n N_C$. The first factor can be ignored, taking into account that the concentration of electrons

at the interface is inverse proportional to the current channel. The second factor can be accounted by estimating the temperature dependence of the mobility as follows:

$$\mu_{eff} = \mu_0 \left(\frac{300}{T}\right)^{3/2} \tag{7.6}$$

where $\mu_0 = \mu_{eff}(300)$.

The third factor we take into account as follows: $C_n N_C \sim T^2$.

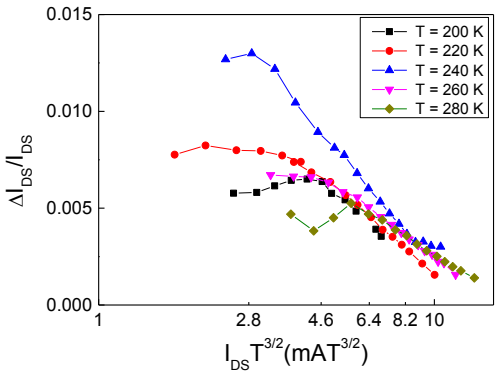


Figure 7.8 Dependence of the normalized amplitude of RTS noise as a function of $I_{DS}T^{3/2}$ measured at different temperatures.

Therefore, Figure 7.5 - Figure 7.7 can be plotted as a function of argument $I_{DS}T^{3/2}$ (Figure 7.8 - Figure 7.10) and following values $\tau_e T^2$ and $\tau_c T^2$ are suitable to be considered instead the time constant values.

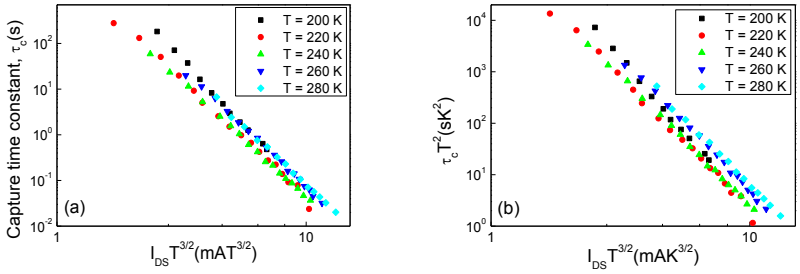


Figure 7.9 Dependence of the time constant of the capture τ_c (a) and value $\tau_c T^2$ (b) as a function of $I_{DS}T^{3/2}$ measured at different temperatures.

Decrease in the relative amplitude of RTS noise in strong inversion confirms the model of Coulomb blockade [129, 130]. According to the model increase in the concentration of free carriers leads to a strong screening of the charge trapped in the center of the dielectric.

Increase of the degree of screening results in the reducing of the magnitude of modulation of the channel current.

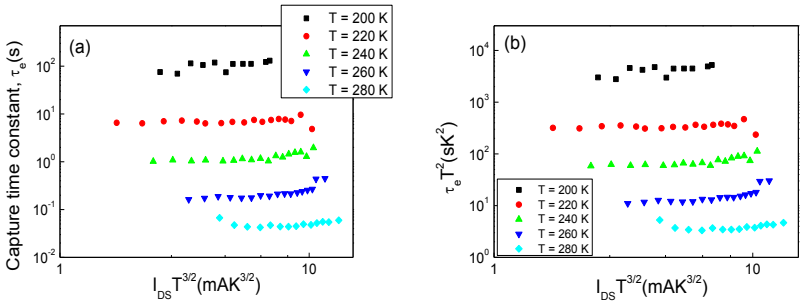


Figure 7.10 Dependence of the time constant of the capture τ_e (a) and value $\tau_e T^2$ (b) as a function of $I_{DS}T^{3/2}$ measured at different temperatures.

Taking into account the dependence of the mobility on temperature, it can be obtained that the curves in Figure 7.9 and Figure 7.10 practically coincide.

The almost coincidence of time constants capture τ_c at the same electron densities and different temperatures has not be considered as misleading and does not indicate a lack of τ_c dependence on the temperature. The difference in the values of τ_c at different temperatures is masked by the changes due to transition between the different long-time metastable states. This difference is in the order of magnitude of changes of value τ_c with the temperature changes, which is described in [123] and shown in Figure 7.6.

For further analysis, we plot the dependence $\tau_e/\tau_c = f\left(I_{DS}T^{3/2}\right)$

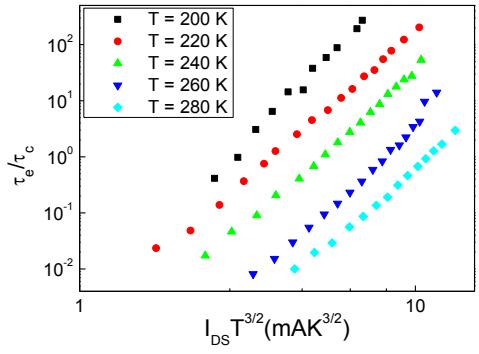


Figure 7.11 Dependence of the ratio of the emission and capture time constants: τ_e/τ_c as a function of the value $I_{DS}T^{3/2}$ measured at different temperatures listed in the figure.

Using data of Figure 7.10 value of energy E_b can be determined by building Arrhenius plot at different temperatures with the parameter $I_{DS}T^{3/2} \sim n$. We assume here that the concentration

of free electrons at the interface n_s is proportional to the average concentration, n. It should be noted that the energy E_b almost unchanged with the change in the value $I_{DS}T^{3/2}$. When $I_{DS}T^{3/2}$ is 6 $mAK^{3/2}$, the temperature dependence of $\tau_e T^2$ can be obtained from Figure 7.10 (b) as show in Figure 7.12, the value of energy can be obtained: E_b = 0.433 eV.

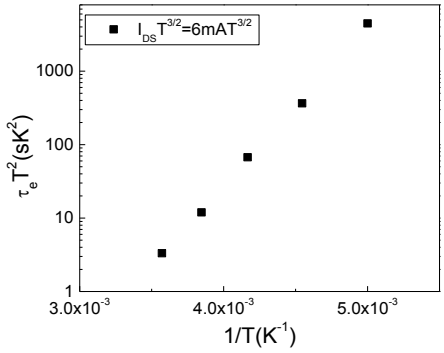


Figure 7.12 Arrhenius plot of $\tau_e T^2$ as a function of 1/*T* extracted from Figure 7.10 (b).

The value of energy ΔE cannot be determined from the temperature dependence of the τ_e/τ_c or τ_c due to the scattering of the data in the temperature measurements. Therefore, we determine the quantity of ΔE using Equation (7.1) and the assumption concerning the electron concentration described above.

The Equation (7.1) can be rewritten as follows:

$$\tau_c = \frac{1}{\sigma_{n0} v_{th} n} exp\left(\frac{\Delta E}{kT}\right) \tag{7.7}$$

Here, the capture cross section is written in the form $\sigma_n = \sigma_{n0} exp(-\Delta E/kT)$ [53, 142], exchange in ΔE is equivalent to changing the capture cross section. This assumption is in agreement with the model of RTS noise, assuming the existence of the Coulomb blockade and the screening potential of the center in the dielectric layer. In the expression for τ_e in Equation (7.2), capture cross section is not affected by the Coulomb blockade, therefore the values of σ_{n0} can be determined by Equation (7.2). To determine this value we calculate the thermal velocity and the density of states at the bottom of the conduction band as follow:

$$v_{th} = \sqrt{\frac{3kT}{m_n^*}} (m_n^* = 1.08\, m_n) \tag{7.8}$$

$$N_c = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2} \tag{7.9}$$

$$\sigma_{n0} = \frac{1}{\tau_e v_{th} N_C} e^{E_b/kT} \tag{7.10}$$

Calculated parameters using Equation (7.10): values of σ_{n0}, v_{th}, N_c obtained at different temperatures are listed in Table 7.1.

Table 7.1 List of evaluated parameters at different temperatures *T*: average thermal velocity v_{th}, Emission time constants τ_e, the density of states at the bottom of the conduction band N_c, and capture cross-section prefactor σ_{n0}.

T(K)	200	220	240	260	280
v_{th}(cm/s)	5.30×10^{6}	5.56×10^{6}	5.81×10^{6}	6.05×10^{6}	6.27×10^{6}
N_c(cm^{-3})	1.53×10^{19}	1.98×10^{19}	2.16×10^{19}	2.26×10^{19}	2.53×10^{19}
τ_e(s)	0.11179	0.00754	0.00117	1.77065×10^{-4}	4.23881×10^{-5}
σ_{n0}(cm^2)	8.77854×10^{-15}	9.78176×10^{-15}	8.27844×10^{-15}	1.00283×10^{-14}	9.09175×10^{-15}

Further, in accordance with Equation (7.7), we calculate the value of ΔE for all points where values τ_e and τ_c were measured. To do this, we calculate the concentration of electrons in the channel. Considering the distribution of electrons across the channel thickness and taking into account Equation (7.6), we determine the concentration of electrons in the following way:

$$n = \left(eR\mu_0\left(\frac{300}{T}\right)^{3/2}\right)^{-1} L/Wd \tag{7.11}$$

where *L*, *W*, *d* are the length, width and thickness of the sample, respectively; *R* is the resistance of the channel.

We used typical value of mobility, μ_0, for our samples, equal to value of 300 cm^2/Vs at 300 K.

The values of the energy of the Coulomb blockade as a function of carrier density are shown in Figure 7.13 and as a function of temperature in Figure 7.14.

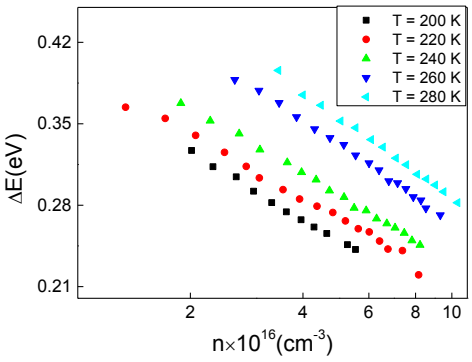


Figure 7.13 The energy of Coulomb blockade as a function of the average electron concentration in the channel obtained at different temperatures.

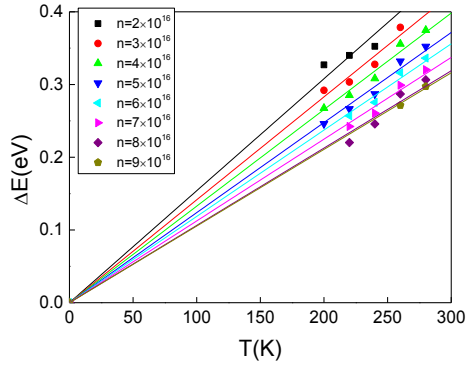


Figure 7.14 Dependence of the values of the Coulomb blockade energy as a function of the temperature. Straight lines are built in accordance with Equation (7.12).

Values of Coulomb energy are in good agreement with the with the values obtained in Ref. [123]. Temperature dependence of ΔE are shown in Figure 7.14, where the line shows the dependencies:

$$\Delta E = -aTln\left(\frac{n}{n_0}\right) \tag{7.12}$$

Figure 7.15 shows normalized temperature Coulomb energy as a function of carrier density, it is represented as follow equation:

$$\frac{\Delta E}{T} = -aln\left(\frac{n}{n_0}\right) \tag{7.13}$$

Where $a = 3.45 \times 10^{-4}$, $n_0 = 1.6 \times 10^{18}\,cm^{-3}$ can be obtained from Figure 7.15. The data are in good agreement with predicted by the model proposed in [123].

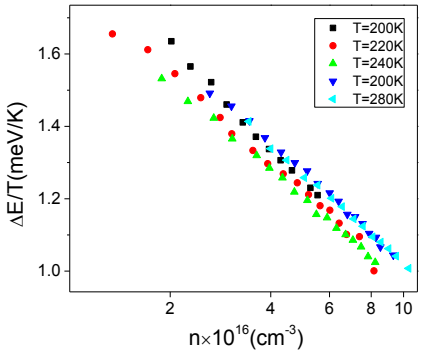


Figure 7.15 Temperature normalized Coulomb free energy as a function of the average electron concentration in the channel obtained at different temperatures.

7.3 Summary

Sub-µm size backgate FETs were fabricated using novel nanoimprint lithography combined with TMAH etching techniques. RTSs at different temperature from 200 K to 280 K were registered in such device, the Coulomb Blockade energy involved during trapping and detrapping of an elementary charge to an interface trap is studied. The results exhibit a deviation of the single interface trap behavior from the classical Shockley-Read-Hall laws. The difference can predominantly be explained by accountancy of the Coulomb Blockade energy, which is linearly proportional to temperature and decreases logarithmically with inversion carrier density in the channel due to screening effect.

As presented in Chapter 6, the deviation from the behavior classically predicted by the Shockley-Reed-Hall theory can be explained by the Coulomb Blockade energy. This Chapter fully characterized this effect by investigating the temperature and charge number dependence over a range of gate voltages. The obtained results allowed us to formulate a well-developed framework to approach the use of RTS phenomena as an alternative sensing technique. The principles outlined above will be revisited in the new utilization of RTS spectra described in Chapter 10.

8. Noise Properties, Sensitivity Limits and Size Dependence of Si NW FET Biochemical Sensors with Micrometer Channels

In this chapter, new Si NW FET array devices were successfully established for biosensing applications. The new process is suitable for mass production, as well as increasing the reliability and reproducibility of the devices. The process demonstrated is based on nanoimprint lithography and wet anisotropic etching of Si by TMAH. The electrical properties of these devices are characterized. Finally, these liquid gated devices are characterized for their minimum charge limit detection.

8.1 Experimental Details

We designed and fabricated Si NW structures with different length and width in order to investigate the effect of the nanostructure scalability on the device performance. The optimized nanoimprint technology was used to transfer the designed pattern to SOI wafer with 37 nm SiO_2 mask layer. These structures were then transferred to the active Si layer by anisotropic wet etching with TMAH. After the TMAH etching, the mask oxide was removed by wet etching. Boron ions (1×10^{15} cm^{-2}) were implanted to the conducting lines of the sensors with energy of 7 keV and were subsequently annealed at 1000 °C for 5 sec in nitrogen atmosphere to reduce serial resistance and improve the electrical performance of the devices. A 6 nm silicon oxide layer was grown using dry oxidation. Afterwards a 6 nm Al_2O_3 layer was deposited using the ALD machine. Stack of both layers served as a gate layer of effective silicon oxide thickness of 9 nm. Metallization was formed using aluminum deposition and lift-off process. In order to lower the contact resistance between the Al and the doped Si, annealing was carried out for 10 min at 400 °C in forming gas (H_2/N_2) atmosphere. At last, SU8 was used as the passivation layer to isolate the metal electrodes from the aqueous medium. The detailed design and the fabrication processes can be found in Chapter 4.4 and Appendix B.3.

The fabricated wafer are shown in Figure 8.1 (a), the red panel shows the individual device cell, after cutting, in order to be characterized in liquid environment, devices were wire bonded on 68-pin LCC carriers (LCC0850, Spectrum, USA) and encapsulated using glass rings and PDMS (Figure 8.1 (b)). One of the device cell was shown in Figure 8.1 (c), the amplified Nanowire picture was shown in Figure 8.1 (d). The SEM pictures demonstrate that the NIL technology is successfully and well developed, it can fabricate the Si NW FET devices with 100% yield and high resolution.

The electrical properties of the backgate and liquid gate nanowire FETs are characterized by I_{DS}-V_G measurements and noise spectroscopy, a powerful tool for investigation of device performance and quality.

The electric properties of Si NW FET sensors were characterized by using a Süss probe station inside of a faraday cage equipped with a Keithley 4200-SCS semiconductor characterization

system. The source was connected to ground. The drain was biased to different voltages, V_{DS}. The back gate contact was realized as an opening in the BOX layer on the front side of the chip and further deposition of the bond pad metal.

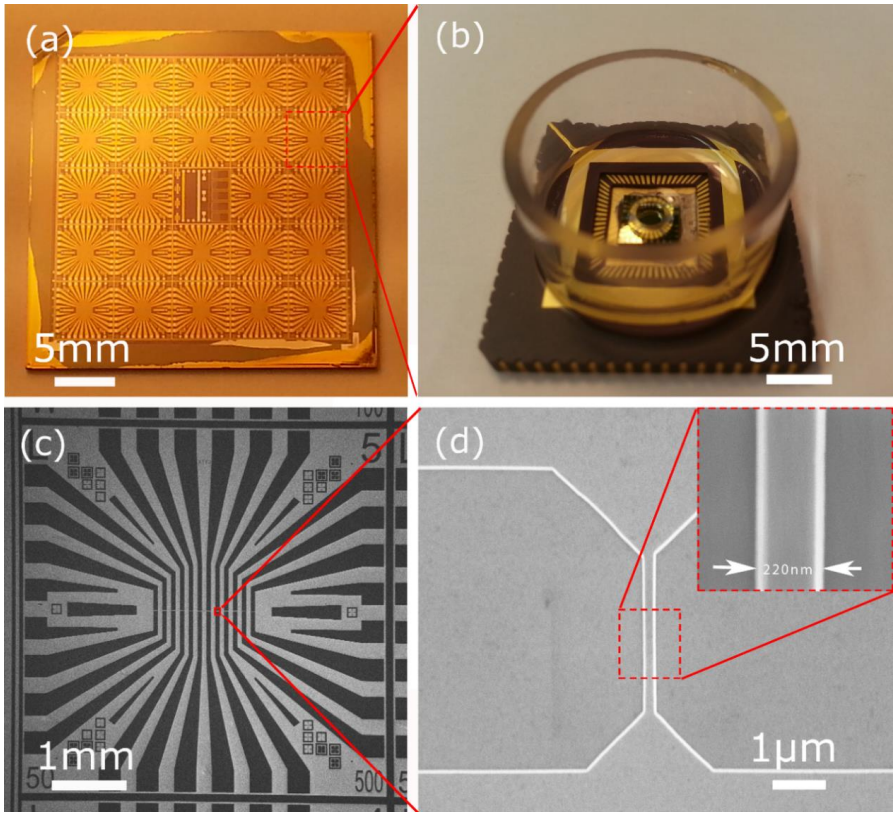


Figure 8.1 (a) Images of fabricated devices using T-NIL, the red panel (field of view: 5 × 5 mm²) indicates the individual device cell. (b) Images of encapsulated sensor from the fabricated devices. (c) SEM picture of one of the device cell. (d) SEM picture of the Si NW. Inset: enlarged SEM picture of the nanowire.

The activation of the silicon oxide surface was performed in oxygen plasma. For silanization the chips were transferred to the glove box containing an argon atmosphere. Silanization with APTES was performed for 1 h inside of a desiccator. A drop of pure APTES was placed inside the desiccator and the whole system was evacuated.

The devices were electrochemically characterized in a 10 mM/L phosphate buffer solution, adjusted to pH 7.4. The pH measurements were performed in 100 mM/L phosphate buffer solution from pH 5 to pH 8.5.

8.2 Results and Discussion

8.2.1 Electrical Measurements of Fabricated Si NW FETs

8.2.1.1 Backgate Device Characteristics

DC characteristics for one of the Si NW devices with backgate are shown in Figure 8.2, the device length is 20 µm and width is 250 nm. The output characteristics were recorded by sweeping of V_{DS} from -3 V to 0 V at different V_{BG} values from 4 V to -2 V with the step of -2 V (shown in different colors) are presented in Figure 8.2 (a). Figure 8.2 (b) shows the transfer characteristics in both linear scale and logarithmic scale were carried out by sweeping V_{BG} from -1 V to 6 V at a constant V_{DS} voltage from -0.1 V to -1.1 V with the step of -0.2 V. The subthreshold slope for the structure was 250 mV/decade which is very low compared to the reported works [141], it demonstrates that our devices have much lower trap density.

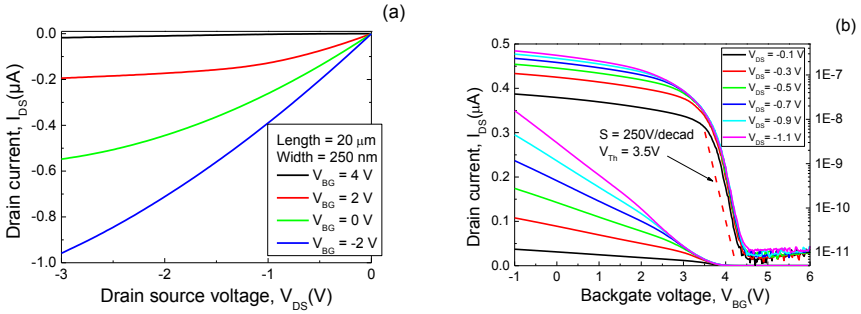


Figure 8.2 Output (a) and transfer (b) characteristics of backgate nanowire FET with W = 250 nm and L = 20 µm.

8.2.1.2 Front Gate Characteristics

The front gate voltage (V_{GS}) was applied through an electrochemical reference electrode immersed into the electrolyte solution. All the results shown in this section are performed in the same conditions (PBS (10 mM), pH 7.4). The backgate was not connected during these measurements.

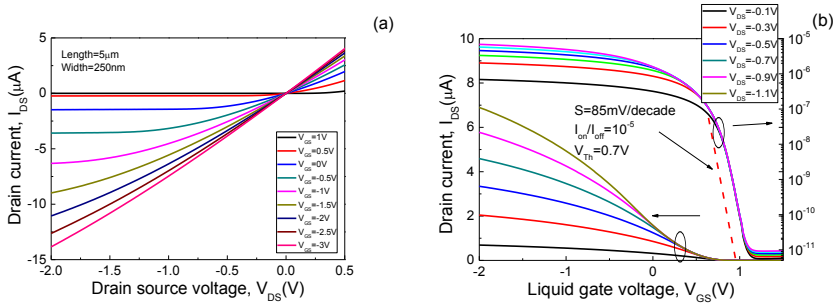


Figure 8.3 Output (a) and transfer (b) characteristics of backgate NW FETs with width = 250 nm and length = 5 µm.

Figure 8.3 (a) shows the output characteristics of the Si NW chips with a wire width of 250 nm and a length of 5 µm. The V_{DS} voltage was swept from -2 V to 1 V and the V_{GS} voltage was applied from -1.5 V to -3.0 V in steps of -0.5 V. Figure 8.3 (b) shows the transfer characteristic of the Si NW devices in linear scale and logarithmic scale. The V_{GS} voltage was swept from 0 V to -3 V and the V_{DS} voltage was varied from -0.5 V to -1.5 V in steps of -0.5 V. The Si NW FETs presented p-channel depletion transistors and had the V_{Th} of about 0.7 V. The subthreshold slope extracted from the transfer-characteristic curve in the logarithmic scale is 85 mV/decade. The p-channel depletion mode of the devices is a result of the depleted charge carriers in the Si NW due to fixed charges at the oxide layers.

8.2.1.3 Characteristics Comparison between Back Gate and Top Gate

The transfer characteristics of transistors in linear scale and log scale with different wire dimensions fabricated on one chip from back gate and top gate are shown in Figure 8.4. In back gate configuration, the threshold voltages were in the range from 1 V to 5V shown in Figure 8.4 (a). But in liquid gate configuration, the threshold voltages are almost the same shown in Figure 8.4 (b).

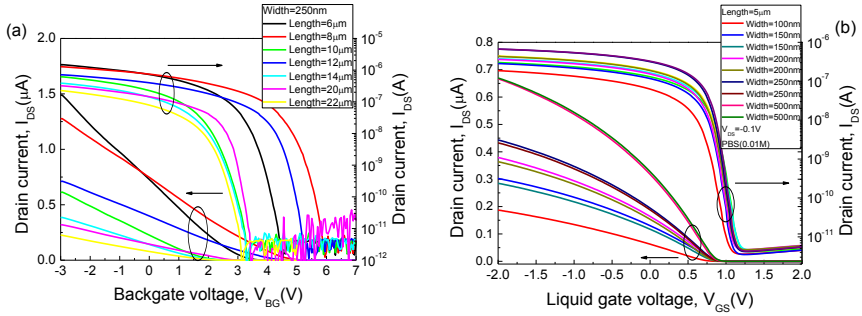


Figure 8.4 (a) Back gate transfer characteristic of the Si NW FETs chips with different wire length. (a) Front gate transfer characteristic of the Si NW FETs chips with different wire width.

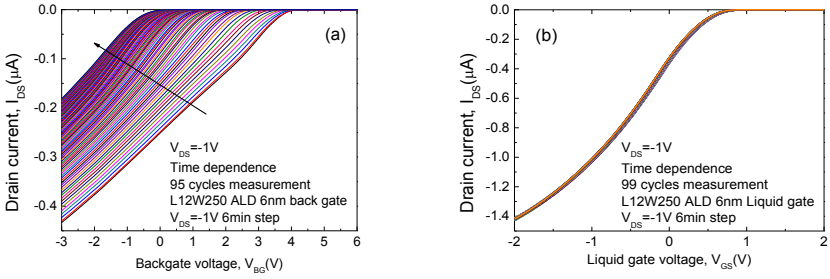


Figure 8.5 (a) Back gate transfer characteristic of the Si NW chips with length = 12 µm, width = 250 nm, the measurements last 9 hours and 95 circles for 6 min after each measurement. (b) Front gate transfer characteristic of the Si NW chips with length = 12 µm, width = 250 nm, V_{DS} = -1 V, the measurements last 9 hours and 99 circles for 6 min after each measurement.

Figure 8.5 (a) and (b) show backgate and front gate transfer characteristic of a Si NW FET with 12 µm length and 250 nm width with 95 cycles during 9 hours, for each measurement with 6 minutes interval. We can find that the threshold voltage of backgate transfer characteristics changes with the time (Figure 8.5 (b)) and the threshold voltage of front gate transfer characteristics change is negligibly small during the whole time of measurement (Figure 8.5 (b)).

We suggest that the reason why the backgate devices have a larger threshold voltage fluctuation is due to the adsorption of charged molecules from the environments on the Al_2O_3 surface, the thereshold voltage fluctuation is proportional to the number of the number of charged molecules. When adding of the electrolyte to the surface of the nanowire, the Al_2O_3 layer absorb the charged molecules on the surface, however, in this case, the thereshold voltage fluctuation is exponential to the number of charged molecules (Chapter 2.2). So the backgate devices have a much higher threshold voltage fluctuation than the liquid gate devices (Figure 8.5). The second reason could be the charging effect, the slow traps hidden in the top dielectric layer of the nanowire get charged with extremely large time constant (about several hours). We assume that the change, ΔQ, of the charge which induces the fluctuation of the threshold voltage ΔV_{Th}. The changing of the V_{TH} can be calculated using the capacitance of the top or bottom dielectric layer, C_{ox}:

$$\Delta V_{Th} = \frac{\Delta Q}{C_{ox}} \tag{8.1}$$

the ΔV_{Th} is inverse proportional to the capacitance of the gate electrode. The capacitance of front gate is much larger than the capacitance of backgate, thus the fluctuation of the threshold voltage of backgate will be bigger than for the front gate (Figure 8.5).

Therefore, the back-gate operation experiences systematic shift in time. This leads to a potential error which might occur during long term measurements. Thus from above described results, it indicate that the utilization of front gate configuration is better than the use of front gate one.

In the experiments, front gate voltage was used, the potential of the backgate was floating (electrode not connected to ground), but the potential of the back gate can influence the operation of the transistor with the front gate. Therefore it is necessary to study the electrical characteristics using both gates and consider coupling between back gate and front gate.

The influence of the back gate voltage onto the front-gate transfer characteristics of single Si NWs (250 nm width and 20 µm) is shown in Figure 8.6. The back gate was biased from V_{BG} = 4 V to V_{BG} = -4 V with -2 V/step. At V_{BG} = 4 V, as we can see the back gate voltage changes the threshold voltage in the case of front gate configuration. It is known as the effect of front and back gate coupling, which was observed previously in case of MOSFET [82, 118].

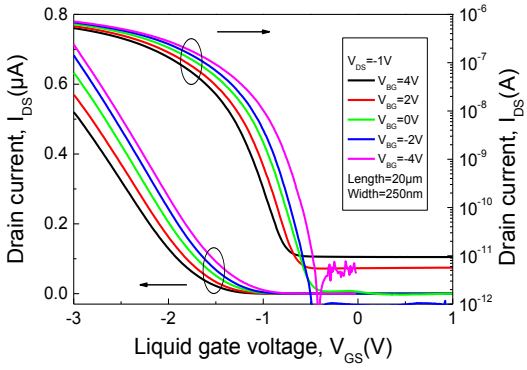


Figure 8.6 Transfer characteristic of Si NW FET as a function of front-gate voltage, measured at different back-gate voltages.

8.2.2 pH Sensitivity of the Si NW FETs

In order to investigate the pH sensitivity of the Si NWs with and without (3-Aminopropyl)triethoxysilane (APTES) modification, APTES is an aminosilane frequently used in the process of silanization, the surfaces are functionalized with alkoxysilane molecules. The transfer characteristics were measured at different pH of electrolyte buffer solutions, the pH solution was changed using a pump.

The typical transfer characteristics of a p-channel Si NW FET with and without APTES modification measured with different solutions of pH values are shown in Figure 8.7 (a) and (b) in logarithmic scales. In both cases, the transfer characteristics shifted to higher front gate voltages (from the left to the right) with increase of the pH-value of the solution. This effect can be explained by the change of the flat-band voltage of the Si NWs caused by the change of the surface charges at the oxide-electrolyte interface terminating in -SiOH or -NH_2 groups [8].

At high pH, without any modification, -SiOH is deprotonated to -SiO^-, which correspondingly causes an increase in conductance. The observed linear response can be attributed to an approximately exponential change in the total surface charge density (versus pH) because of the combined acid and base behavior of both surface groups.

Considering the surface functionality of the modified Si NWs. Si NW oxide surface is covalently linked with APTES to results in a surface terminating with -NH_2 groups in the solution. At low pH, the -NH_2 group is protonated to -NH_3^+ [143] and acts as a positive gate, which depletes hole carriers in the p-type Si NW and decreases the conductance.

Figure 8.7(c) shows the threshold voltage shift with pH values extracted from the data shown in Figure 8.7 (a) and (b). The shifting of the flat-band voltage extracted from the transfer characteristics curves were approximately 33 mV/pH and 41 mV/pH. This demonstrate that the Si NWs with modification have higher sensitivity with hydrogen ions in the solution.

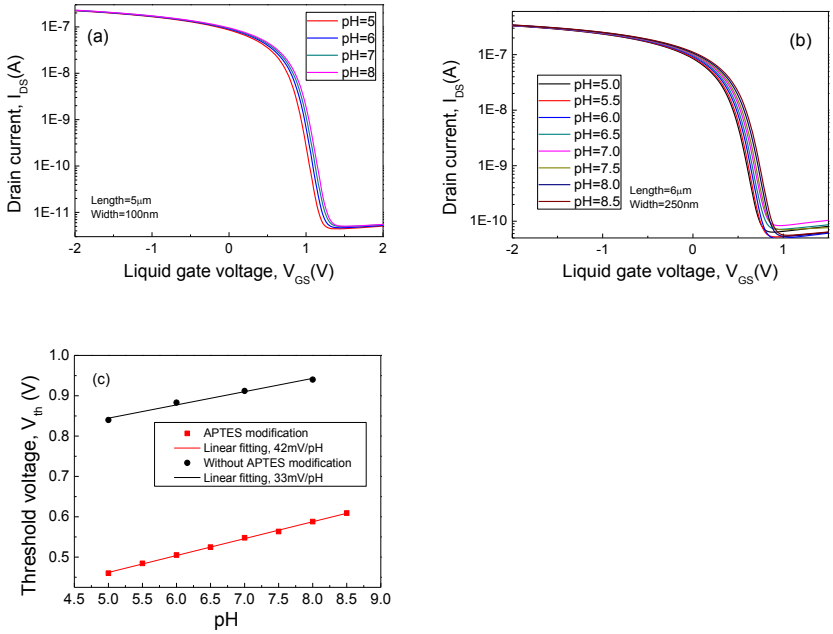


Figure 8.7 (a) Transfer characteristics of a p-type Si NW transistor without any modification measured with different pH-values solutions in logarithmic scale. (b) Transfer characteristics of a p-type Si NW transistor modified with APTES measured with different pH-values solutions in logarithmic scale. (c) Threshold voltage shift as a function of pH values extracted from the data shown in (a) and (b).

8.2.3 Low-frequency Noise Characteristics of the Si NW FETs

In order to study the dimension dependence of transport performance of Si NW FETs sensor, the current-voltage and noise characteristics of Si NW FETs with different channel length from 2 μm to 22 μm with the same width of 250 nm and different channel width from 100 nm to 500 nm with the same length of 5 μm were measured at different gate voltages with the constant drain voltage of -100 mV.

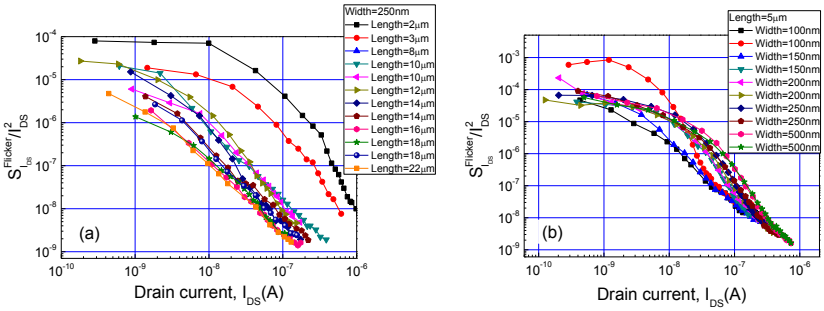


Figure 8.8 Drain current dependence of the drain current PSD at 1 Hz of different channel length (a) and width (b) of Si NW FET devices. Nanowire length ranges from 2µm to 22 µm and width ranges from 100 nm to 500 nm.

The normalized current noise power spectra of flicker noise, S_I/I^2, as a function of drain current at 1 Hz of different channel dimension of Si NW FET devices as shown in Figure 8.8.

One of the traditional transfer characteristics and the corresponding transconductance of Si NW FET with channel length of 5 µm and width of 150 nm is shown in Figure 8.9.

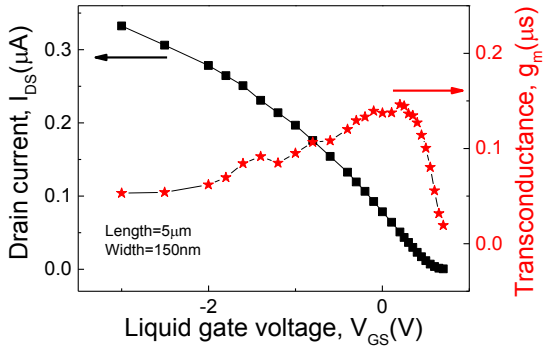


Figure 8.9 Transfer characteristics (black) and the corresponding transconductance (red) of liquid gated Si NW FET with length = 5 µm, width = 150 nm at V_{DS} = -100 mV.

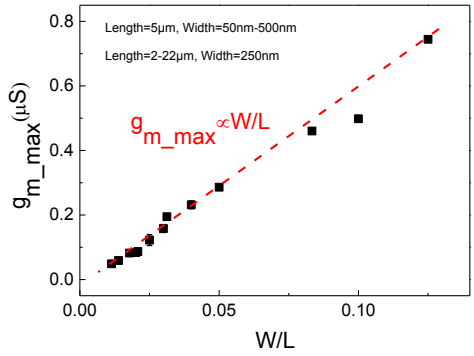


Figure 8.10 Peak transconductance (g_{m_max}) as a function of *W/L*, dashed line indicates linear fitting of the plots. NW length ranges from 2 µm to 22 µm and width ranges from 100 nm to 500 nm.

The maximum of transconductance, g_m, is found from

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{8.2}$$

For a FET with a long enough channel and in its linear working region, the intrinsic transconductance can be expressed as [20]:

$$g_m = \mu_{eff} C_{ox} \frac{W}{L} V_{DS} \tag{8.3}$$

where μ_{eff} is the effective mobility of the charged carriers, C_{ox} is the oxide capacitance per unit area, W is the width of the nanowire channel and L is the length of the NW channel. Basing on this equation we can conclude that the maxmum transconductance, g_{m_max}, is inverse proportional to the length of the NW and proportional to width, which are consistent with our measurement results shown in Figure 8.10.

The effective mobility μ_{eff} of the Si NW FETs can be estimated using the following equation for long-channel FETs at low drain-source voltage from Equation (8.3):

$$\mu_{eff} = \frac{L_{DS} g_m}{W C_{ox} V_{DS}} \tag{8.4}$$

where $C_{ox} = \varepsilon_r \varepsilon_0 / d$ is the gate capacitance, L_{DS} is the transistor channel length, W is the width of the channel, V_{DS} is the drain-source voltage, ε_r is the dielectric constant of SiO_2, t is the equipment thickness of the SiO_2 layer. Using ε_r = 3.9, t = 9.8 nm, V_{DS} = 100 mV and insert the maxmum transconductance, $g_{m\_max,}$ from Figure 8.10, we obtain the peak mobility as shown in Figure 8.11 (a) and (b), which is comparable with the reported results [23] for p channel Si NW FET biosensor.

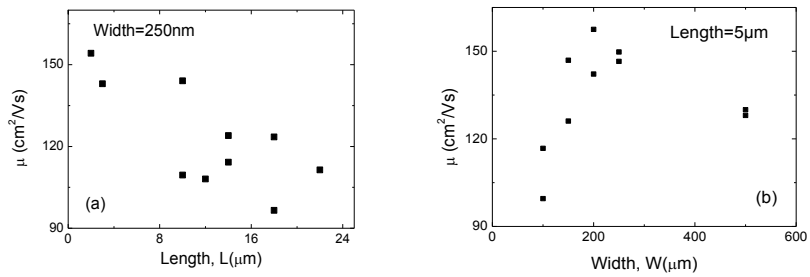


Figure 8.11 Peak mobility (μ_{eff}) of different channel length (a) and width (b) of Si NW FET devices. NW length ranges from 2μm to 22 μm and width ranges from 100 nm to 500 nm.

In order to compare the noise level of our devices with reported noise values in literature, we estimated the Hooge's parameters using Hooge's empirical model [25]:

$$\frac{S_I}{I_{DS}^2} = \frac{\alpha_H}{fN} \tag{8.5}$$

where N is the number of carriers and α_H is the Hooge's constant, which is used to quantitatively assess and compare the noise performance of our devices.

The drain current (I_{DS}) in the linear regime follows Ohm's law, it can be expressed as

$$I_{DS} = nq\mu_{eff}EWh \tag{8.6}$$

where q is the elementary charge, E is the electric field, n and μ_{eff} is the concentration of carriers in the conducting channel of the NW FET and carrier mobility, respectively. The concentration can be expressed as N/V, where N is the total number of carriers, $V = W \times L \times h$ is the volume of the NW channel. Here W is the width of the NW channel, h is the heigth, L is the length of the NW channel. E equals V_{DS}/L.

The total number of carriers, N, in the working point with the maximum of the transconductance is caculated using the following equation:

$$N = \frac{I_{DS}L^2}{qV_{DS}\mu_{eff}} \tag{8.7}$$

Then we insert this equation into the definition of flicker noise in Equation (8.5), the Hooge's constant, α_H, can be expressed as:

$$\alpha_H = \frac{fS_I}{I_{DS}^2} \cdot \frac{I_{DS}L^2}{qV_{DS}\mu_{eff}} \tag{8.8}$$

And thus we obtain the Hooge's constant, which is shown in Figure 8.12 (a) and (b) for different NW geometries. α_H exhibits a minimum value of 6.9×10^{-4} and an average value of 1.6×10^{-3}, which is lower than values reported for traditional EBL-processed samples [26].

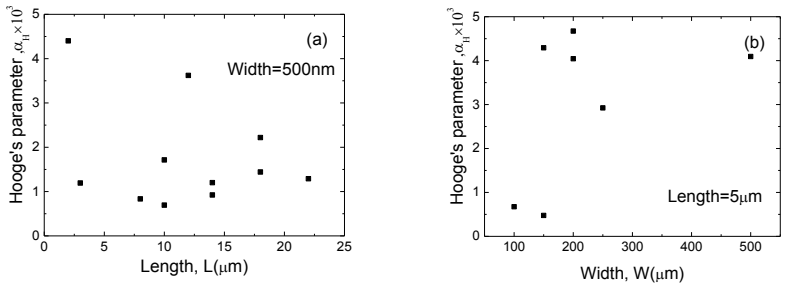


Figure 8.12 Hooge's constants are estimated using measured noise spectra data as a function of channel length (a) and width (b) of Si NW FET devices. Nanowire length ranges from 2 µm to 22 µm and width ranges from 100 nm to 500 nm. Measurement error of noise spectral density is about 10%.

The 1/*f* noise in the drain current can be transformed to an equivalent input gate voltage noise (S_U) which is calculated from the drain current noise using

$$S_U = \frac{S_I}{{g_m}^2} \tag{8.9}$$

where S_I is the drain current noise spectral density.

Figure 8.13 shows the transconductance and equivalent input gate voltage as functions of drain current, obviously, at the maximum transconductance, it has a minimum equivalent input gate voltage. So this give us the idea to set our work point during the Si NW FET biosensor applications, it is better to choose the maximum transcuctance point, because it has a higher amplification capability and lower equivalent input gate voltage.

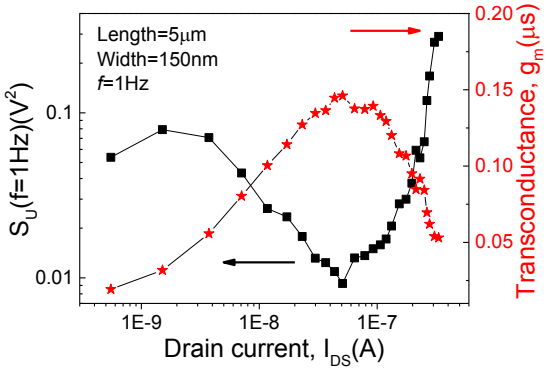


Figure 8.13 Equivalent input gate voltage noise (black curve, f = 1 Hz) and transconductance (red curve) of liquid gated Si NW FET (length = 5 μm, width = 150 nm) plotted on logarithmic and linear scales at V_{DS} = -100 mV.

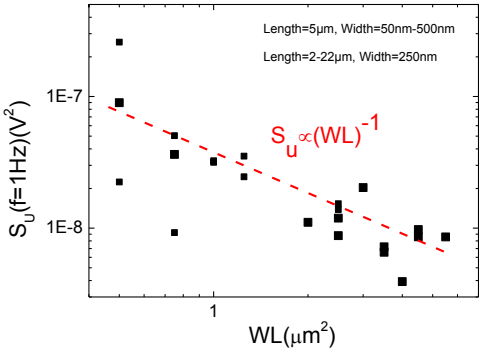


Figure 8.14 Equivalent input gate voltage noise (f = 1 Hz) calculated using noise spectra data as a function of surface area (WL), the dashed line shows the fit to the data, $S_U \propto 1/WL$, measurement error of noise spectral density is about 10 %. Nanowire length ranges from 2 μm to 22 μm and width ranges from 100 nm to 500 nm.

For a negligible scattering coefficient, in the linear regime of operation, $S_U = S_{VFB}$ [27]. Gate voltage noise is important in the case of measurements of threshold voltage shifts and is minimized in the region of peak transconductance. The S_{VFB} can be expressed as [144]

$$S_{VFB} = \frac{\lambda KTq^2 N_t}{fWLC_{ox}^2} \tag{8.10}$$

where k is the tunneling attenuation distance, W is the width, L is the length, C_{ox} is the capacitance per unit area, q is the electronic charge, k is the Boltzmann constant, T is absolute temperature, and N_t is the trap density. From Equation (8.10), we can derive $S_U \propto 1/WL$, this is consistent with S_U (f = 1Hz) deduced from Equation (8.9) find in Figure 8.14.

8.2.4 Sensitivity of Biosensor

One dimension FET biosensors have shown great sensitivity when employed as biological/chemical biosensor, especially single-molecule detection of DNA [145, 146] and Single-Molecule Protein with Carbon Nanotube Field-Effect Sensors [147] as well as single viruses with Si NW field effect transistors [16]. However, the sensing capability of the FET sensor is determined by the noise of the FET device, which is determined by the size of the device. So it is necessary to study the size dependence of minimum number of detectable charges on Si NW FET sensor.

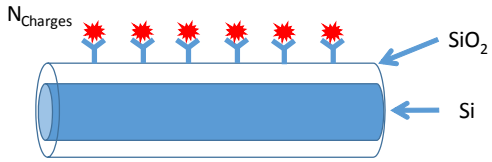


Figure 8.15 Schematic of a nanowire device configured as a sensor with receptors and binding of charged molecules (red).

During the sensor activity, the change of the surface potential $\Delta\psi_0$, caused by surface event (e.g. action potential of a cell on top of the NW or binding of the analyte to the surface of the sensor) shown in Figure 8.15 is registered a change of drain current δI, which can be expressed as superposition of useful signal δI_S and fluctuations caused δI_{fl}:

$$\delta I = \delta I_S + \delta I_{fl} \tag{8.11}$$

Signal-to-noise ratio (SNR) is defined as:

$$SNR = \frac{\delta I_S}{\delta I_{fl}} \tag{8.12}$$

The measured signal response (δI_s) is given by the change in surface potential ($\Delta\psi_0$) multiplied by the transconductance (g_m)

$$\delta I_S = \Delta\psi_0 \cdot g_m(V_G) \tag{8.13}$$

where g_m is the transconductance of the transistor in response to the variation of liquid-gate voltage (V_{GS}) at the applied bias voltage (V_{DS}).

The root-mean-square (rms) current noise amplitude (δI_{fl}) is obtained by integrating S_I over the measurement bandwidth and taking the square root:

$$\delta I_{fl} = \sqrt{\int_{f_1}^{f_2} S_{I_{fl}} df} \tag{8.14}$$

In low frequency region, the main component of the noise is flicker noise which is $1/f$ noise, so in low frequency Equation (8.14) can be deduced as

$$\delta I_{fl} = \sqrt{\int_{f_1}^{f_2} S_{I_{fl}} df} = \sqrt{BW'} \cdot \sqrt{S_{I_{flicker}}(f = 1Hz)} \tag{8.15}$$

where BW′ = ln(f_2/f_1) for low frequency cutoff f_1 and high frequency cutoff f_2 in the measurement bandwidth.

Input Equation (8.9), Equation (8.13) and Equation (8.15) to Equation (8.12), we get:

$$SNR = \frac{\delta I_S}{\delta I_{fl}} = \frac{\Delta\psi_0}{\sqrt{BW'}} \frac{g_m(V_g)}{\sqrt{S_{I_{flicker}}(f = 1Hz)}} = \frac{\Delta\psi_0}{\sqrt{S_U(f = 1Hz)}\sqrt{BW'}} \tag{8.16}$$

In order to calculate the minimum detectable charges using Si NW FET sensor. We assume the minimum SNR to be 1, $\Delta\psi_0 = N_{Charges}q/C_{OX}WL$, where $N_{Charges}$ is the charges can be detected. We put the value of $\Delta\psi_0$ to Equation (8.16) and consider that f_1 = 1 Hz and f_2 = 10kHz, BW' = ln(f_2/f_1) = 9.21, we can get

$$N_{Charges} = \frac{C_{ox}WL\sqrt{S_U(f = 1Hz)}\sqrt{BW'}}{q} \tag{8.17}$$

From above Equation (8.17), as $S_U \propto 1/WL$, then $N_{Charges} \propto (WL)^{0.5}$ which is consistent with the value from our measurement results shown in Figure 8.16. the red fitting line indicate that the number ($N_{Charges}$) of detectable minimum charges on Si NW FET sensor of Si NW FET sensor increases proportionally with the square root of channel surface area (WL) shown in Figure 8.16. This result indicates that the minimum number of detectable charges to be around 8 elementary charges for our bio-FETs with 5 µm length and 100 nm width, taking into account measurement error of noise spectral density (about 10%) and approximation dependence (red dashed line).

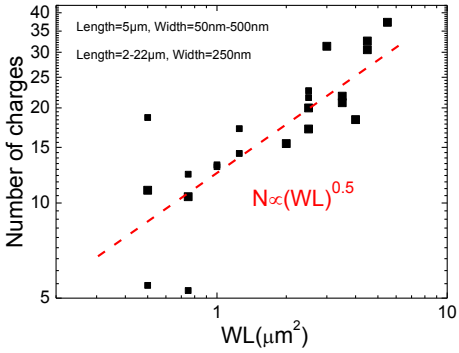


Figure 8.16 Minimum number of detectable charges estimated using measured noise spectra as a function of surface area (*WL*), the dashed line shows the fit to the data, $N_{Charges} \propto (WL)^{0.5}$, measurement error of noise spectral density is about 10 %. Nanowire length ranges from 2 µm to 22 µm and width ranges from 100 nm to 500 nm.

8.3 Summary

High quality Si NW FETs biosensor with different width and length have been fabricated using a top-down silicon fabrication technique. It shows stable *I-V* characteristics and the pH sensitivity of the device is 33 mV/pH and 41 mV/pH without APTES modification and with modification, respectively. Low frequency noise of the Si NW FET was measured to investigate the noise behavior and the minimum number of detectable charges of our devices. These results indicate that the number of detectable minimum charges on Si NW FET sensor of Si NW FET sensor increases proportionally with the square root of surface area of the NW. This scaling rule give us the perspective of the design and fabrication of bio sensors with small channels for single molecule detection application.

When scaling down, new features might appear in the transport properties and determining these is the main aim of the next chapter. There we scale the channel down to the submicrometer range and determine the sensitivity of the nanoscale device. Later, in Chapter 10, an additionally revealed RTS component is shown to be very important for biosensing applications in extremely small devices.

9. Transport Properties of Si NW FETs with Submicrometer Channel

Si NW FETs show great sensitivity when employed as biological/chemical sensors and for electrophysiological recordings [8, 19, 23, 24, 148]. A lot of efforts have been devoted to increasing sensitivity (defined as $\Delta I_{DS}/I_{DS}$) which is maximized in subthreshold regime [149]. However, the noise influence on signal to noise ratio (SNR) was neglected, especially for the cell signal capture. In order to know the sensitivity limit of the biosensors, the SNR and the factors which influence the SNR should be well understood.

In this chapter, P type and N type Si NW FETs with different channel dimensions were fabricated. Both I_{DS}-V_{GS} and noise measurements were carried out, the results indicate that the SNR is maximized in the linear regime at the point where the transconductance is largest in long p type channel (more than 1 µm) nanowire FETs, which is in agreement with R. Rajan and M. Reed's work [27] and the results from chapter 8.2.4. However, during p type short channel (less than 1 µm) nanowire FETs and all of n type nanowire FETs, SNRs are independent of liquid gate voltage.

9.1 Experiments Details

9.1.1 Si NW FETs Fabrication

SOI substrate with a low boron doping level of the active layer 10^{15} cm^{-3} was used. At the first, a thin layer of 37 nm SiO_2 was formed by dry oxidation. The layer is used as a mask, to define: Si NWs with contacts using EBL. After this, the structure was transferred from the mask layer by RIE. TMAH anisotropical etching was used to define our nanowire and contact line structures. Boron and arsenic ion implantation were performed to fabricate the source and drain with ohmic contacts to the nanowires, which were protected by hydrogen silsesquioxane (HSQ) resist regions, defined by EBL, during the implantation process. A 9 nm thick gate oxide layer was grown in a thermal furnace at 1000 ℃ as a protection layer for liquid gated measurements. The source/drain contact pads and the backgate electrodes (300 nm Al layers) were formed using conventional lithography, electron-beam evaporation and a lift-off process. Afterwards, annealing was carried out to lower the contact resistance between the Al and the doped Si. The detailed design and fabrication information can be found in Chapter 4.5 and Appendix B.4. Figure 9.1 shows a SEM image of a Si NW FETs device and the magnification image of one Si NWs.

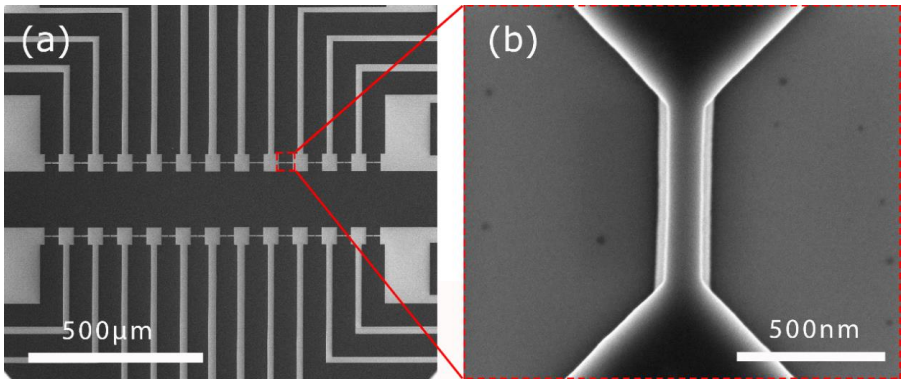


Figure 9.1 SEM image of a Si NW FET device (a) and the enlarged image of the Si NW (b).

9.1.2 Electrical Characterization

P and N type Si NW FETs with single nanowires of 50 nm to 12 µm length and 50 nm to 500 nm width were selected for the DC and low-frequency noise characterization. For the initial measurement, we used a 0.01 M phosphate buffered saline (PBS, Sigma-Aldrich) with pH value of 7.4. The DC characteristics of the devices were measured using a semiconductor parameter analyzer (K4200, Keithely). Low-frequency noise measurements in the frequency range were carried out from 1Hz to 100 kHz using a homemade setup.

9.2 Results and Discussion

9.2.1 Electric Measurements of Si NW FETs

Figure 9.2 shows the drain current (I_{DS}) vs. liquid gate voltage (V_{GS}) characteristics of the Si NW FETs, measured at small drain voltage, V_{DS} = -0.1 V.

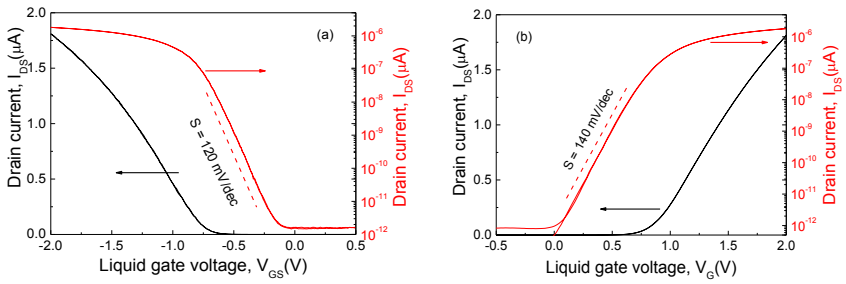


Figure 9.2 I_{DS}-V_{GS} transfer characteristics of P type (a) and N type (b) liquid gated Si NW FET shown in linear (black curve) and logarithmic scale (red curve) at V_{DS} = -0.1 V in 10 mM PBS solution, the NW length is 0.5 µm, width is 200 nm, the Subthreshold slope is close to 120 mV/dec and 140 mV/dec for P-type FET (Fig. 9.2a) and N-type FET (Fig. 9.2b), respectively.

During the measurement of the P-type and N-type Si NW FETs properties, the gate voltage was swept from -2 V to 0.5 V and 2 V to -0.5 V, respectively, the source was grounded, back-gate contact was left floating and the drain-source voltage was kept fixed at -100 mV and 100

mV. The Si NW FETs show high on-off ratio and a low subthreshold slope of 120 mV pro decade and 140 mV pro decade for p and n type devices, respectively. The transfer characteristics with ignored trapping-induced hysteresis shown in Figure 9.2 (a) and (b) suggests a very low equivalent trap density of the devices. These results demonstrate that the fabricated liquid gate FET devices have a high quality which will be very helpful for the biosensor application, the further transport characteristics will be given in this chapter.

9.2.2 Low-frequency Noise Characteristics of the Si NW FETs

9.2.2.1 IV Characteristics

In order to study the dimensions dependence of transport performance of Si NW FETs with accumulation (p type) and inversion (n type) modes, the current-voltage and noise characteristics were carried out at different gate voltages with a constant drain voltage (-100 mV and 100 mV for p and n-types channel, respectively). The channel length range from 50 nm to 12 µm with the same width of 100 nm and width range from 50 nm to 500 nm with the same length of 500 nm.

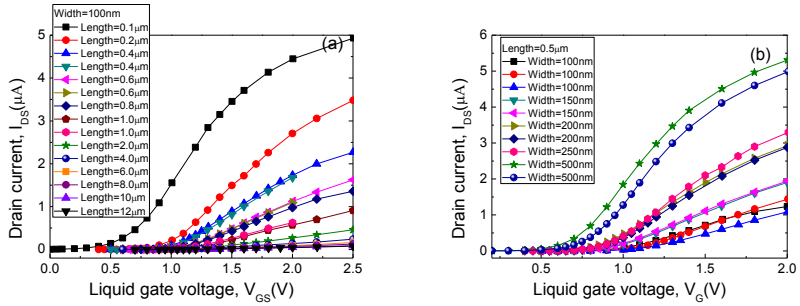


Figure 9.3 (a) Transfer characteristics of samples with different length ranging from 0.1 µm to 12 µm and the same width of 100 nm at V_{DS} = -100 mV. (b) Transfer characteristics of samples with different width ranging from 100 nm to 500 nm and the same length ranging of 0.5 µm at V_{DS} = 100 mV.

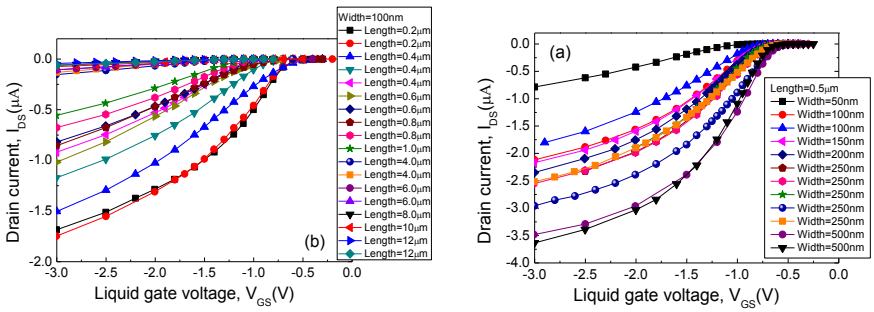


Figure 9.4 (a) Transfer characteristics of samples with different length ranging from 0.1 µm to 12 µm and the same width of 100 nm at V_{DS} = -100 mV. (b) Transfer characteristics of samples with different width ranging from 100 nm to 500 nm and the same length of 0.5 µm at V_{DS} = 100 mV

Figure 9.3 (a) and (b) show transfer characteristics of different channel length ranging from 0.1 µm to 12 µm with the same width of 100 nm and different channel width ranging from 100 nm to 500 nm with the same length of 0.5 µm of the n-type devices.

Similarly, Figure 9.4 (a) and (b) show transfer characteristics of different channel length ranging from 0.1 µm to 12 µm with the same width of 100 nm and different channel width ranging from 100 nm to 500 nm with the same length of 0.5 µm of the p-type sample.

9.2.2.2 Maximum of Transconductance

The maximum of transconductance, g_m, is calculated from each transfer curve using following equation

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{9.1}$$

For a FET with a long enough channel and in its linear working region, the intrinsic transconductance can be expressed as [150]:

$$g_m = \mu_{eff} C_{ox} \frac{W}{L} V_{DS} \tag{9.2}$$

where μ_{eff} is the mobility of the charge carriers, C_{ox} is the oxide capacitance per unit area, W is the width of the NW channel and L is the length of the NW channel, V_{DS} is the drain source voltage, which is kept constant at 0.1 V (n type) and -0.1 V (p type) during the measurements. Basing on this equation, at the maximum value of mobility, we can conclude that the $g_{\mathrm{m\_max}}$ is inverse proportional to the length and is proportional to width of the NW.

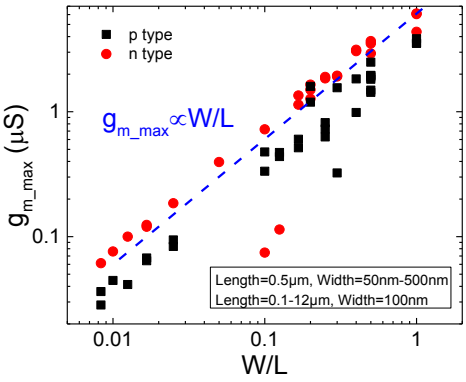


Figure 9.5 Maximum transconductance plotted as a function of *W/L*, showing that Maximum g_m scales with the ratio of *W/L*. Nanowire length ranges from 50 nm to 12 µm and width ranges from 50 nm to 500 nm.

Figure 9.5 shows that the maximum transconductance scales linearly with the ratio of W/L, this result is in agreement with the Equation (9.2). The transconductance of n type devices are a little higher than p type devices, this due to the higher mobility of electrons than holes.

9.2.2.3 Mobility

The effective mobility μ_{eff} of the charge carriers in the NW FET can be estimated using the following equation for long-channel FETs at low drain-source voltage:

$$\mu_{eff} = \frac{Lg_m}{WC_{ox}V_{DS}} \tag{9.3}$$

where $C_{ox} = \varepsilon_r\varepsilon_0/t_{ox}$ is the gate capacitance per unit area, L is the transistor channel length, W is the width of the channel, V_{DS} is the drain source voltage, ε_r is the dielectric constant of SiO_2. Using ε_r = 3.9, t_{ox} = 9.0 nm, V_{DS} = +/-100 mV, we obtain the mobility as shown in Figure 9.6 (a) and (b). These results demonstrate that mobilities of n type and p type devices, with a average value of 200 cm^2/Vs and 100 cm^2/Vs respectively, are independent on the channel dimesnions.

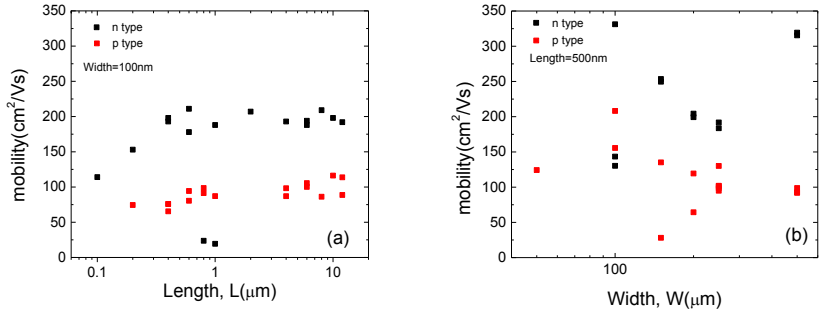


Figure 9.6 Field effect mobility as a function of channel length (a) and channel width (b) in p type (red) and n type (black) Si NW FETs. Nanowire length ranges from 50 nm to 12 µm and width ranges from 50 nm to 500 nm.

9.2.2.4 Threshold Voltage

Threshold voltages (V_{Th}) were extracted by extrapolation of the linear part of the transfer characteristics. Figure 9.7 (a) shows that the threshold voltages are dependent on the channel length when the channel length of the devices goes to submicrometer scale, however, it is almost the same in the devices with micrometers in length. This can be explained by the drain induced barrier lowering effect (DIBL) [151-153].

However, if we have a look at dependence of the threshold voltage on width of the nanowire (Figure 9.7 (b)), it can be clearly seen that narrow nanowire have higher threshold voltages. This is an evidence that the smaller dimension channels have a better electrostatic control of the channel charge carriers and limit short channel effects. Additionally, the interface charges play a bigger role because of bigger surface to volume ration comparing with the wider channel devices. Another effect is that the gate oxide is thicker in average when the diameter

of the wires is smaller. The reason for this is that in smaller wire the (111) plane dominates and the gate oxide growth is faster at the (111) plane than (100) plane. This leads to an increase of the threshold voltage because of thicker average gate oxide layer.

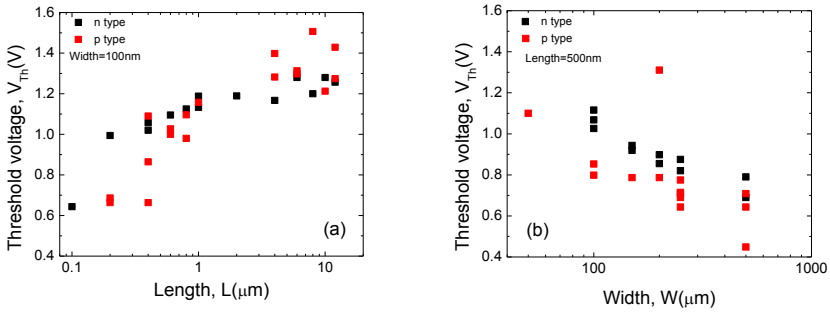


Figure 9.7 Threshold voltages of Si NW FET samples (n type (black) and p type (red)) plotted as a function of channel length (a) and width (b) at V_{DS} = -100 mV. Nanowire length ranges from 50 nm to 12 µm and width ranges from 50 nm to 500 nm.

9.2.2.5 Equivalent input gate voltage noise

Equivalent input gate voltage noise (S_U) is calculated from the drain current spectral density using following equation:

$$S_U = \frac{S_I}{{g_m}^2} \tag{9.4}$$

where S_I is the drain current noise spectral density, g_m is the transconductance calculated from the transfer curves.

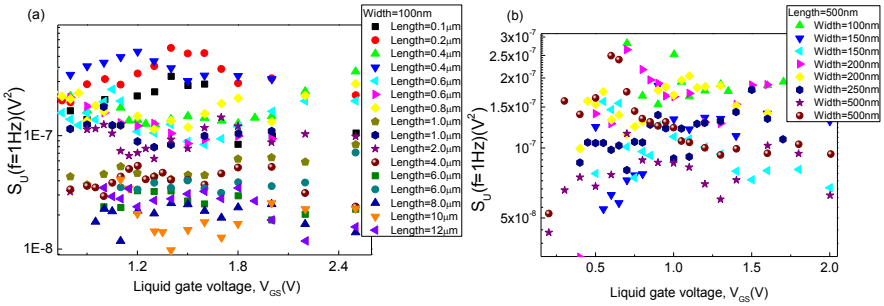


Figure 9.8 Equivalent input gate voltage noise (f = 1 Hz) calculated using measured noise spectra of inversion module devices (n type) as a function of liquid gate voltage. Measurement error of noise spectral density is about 10%. Nanowire length ranges from 100 nm to 12 µm with a width of 100 nm (a) and width ranges from 100 nm to 500 nm with the same length of 500 nm (b).

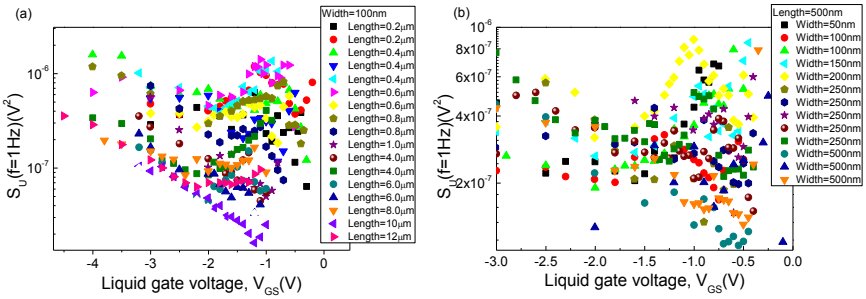


Figure 9.9 Equivalent input gate voltage noise (*f* = 1 Hz) calculated using measured noise spectra of accumulation module devices (p type) as a function of liquid gate voltage. Measurement error of noise spectral density is about 10%. Nanowire length ranges from 200 nm to 12 µm with a width of 100 nm (a) and width ranges from 100 nm to 500 nm with the same length of 500 nm (b).

Figure 9.8 (a) and (b) show the equivalent input gate voltage noise of inversion mode samples with different width ranging from 100 nm to 500 nm and the same length of 0.5 µm at V_{DS} = 100 mV. It is clearly seen that the input referred gate noise values have no dependence on the gate voltage, which indicates, that the flicker noise is mainly generated by the traps in the dielectric layer of the NW and can be explained in frame of number fluctuation model [29].

However, in long channel devices with accumulation mode (p-type channel devices), the equivalent input gate voltage noise is dependent on the gate voltage as shown in Figure 9.9 (a), in short channel devices shown in Figure 9.9 (a) and (b), the equivalent input gate voltage noise remain independent on the gate voltage. These results can be explained that in long channel devices, the mobility fluctuation prevail and when shrink the channel to submicrometer range, the number fluctuation prevail.

For a negligible scattering coefficient, in the linear regime of operation, $S_U = S_{VFB}$ [27]. The S_{VFB} can be expressed as [144]:

$$S_{V_{FB}} = \frac{\lambda KTq^2 N_t}{fWLC_{ox}^2} \tag{9.5}$$

where λ is the tunneling attenuation distance, W is the width, L is the length, C_{ox} is the capacitance per unit area, q is the electron charge, k is the Boltzmann constant, T is absolute temperature, and N_t is the trap density.

Equivalent input gate voltage noise is an important value to compare the amplitude of threshold voltage shifts. In n type inversion mode devices, as S_u does not depend on the gate voltage, it is derived for the averaged value in linear region. On the other hand, in p type accumulation mode, the equivalent input gate voltage noise, S_u, is chosen in the region of maximum transconductance as at this region, it has the minimized value (Figure 9.10).

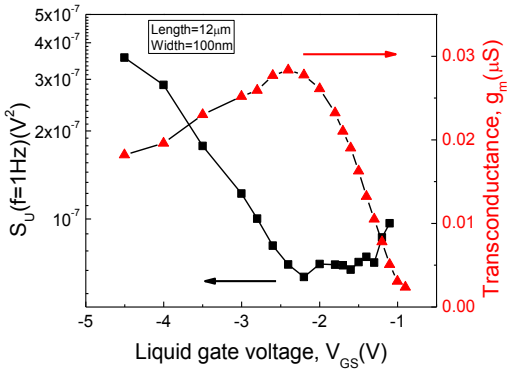


Figure 9.10 Equivalent input gate voltage noise (black) and transconductance (red) as a function of liquid gate voltage, the length is 12 μm and the width is 100 nm.

From Equation (9.5), we can derive that $S_U \propto 1/WL$. This is consistent with S_u taken at f = 1 Hz (Figure 9.11(a) and (b)).

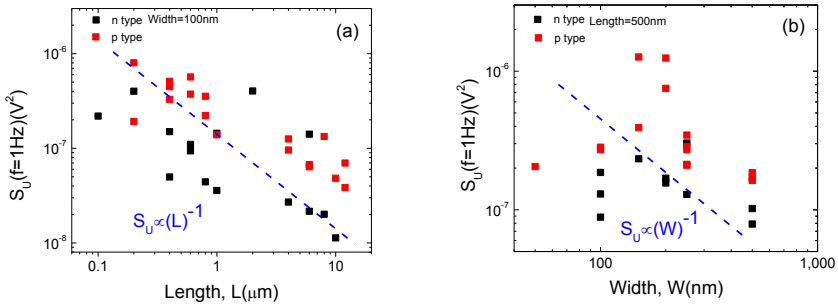


Figure 9.11 Equivalent input gate voltage noise calculated using measured noise spectra as a function of channel length (a) and width (b) of Si NW FET devices, dashed lines show a power law with exponent of -1, measurement error of noise spectral density is about 10%. Nanowire length ranges from 0.1 μm to 12 μm and width ranges from 50 nm to 500 nm.

9.2.2.6 Sensitivity of the Biosensor

As discussed in last chapter, the minimum number of detectable charges using Si NW FET sensor is defined as:

$$N_{Charges} = \frac{C_{ox} WL \sqrt{S_U(f = 1Hz)} \sqrt{BW'}}{q} \tag{9.6}$$

From Equation (8.17), $S_U \propto 1/WL$, we can conclude that $N_{Charges} \propto (WL)^{0.5}$ which correlates with our measurement results shown in Figure 9.12. The red line is the prediction line, which

increases proportionally with the square root of length (Figure 9.12 (a)) or width (Figure 9.12 (b)).

We can find that in Figure 9.12 (a), in short channel device, the number of minimum detectable charges is lower than the prediction. One of the reason is that during the fabrication process, the HSQ pattern was defined by the same dose. However, for small structures, the dose of electron beam should be higher than big structures. It results in the smaller structure of the channel length than what we designed. Therefore the number of minimum detectable charges is lower than what we expected using Equation (9.11). Another reason is that, in smaller channel devices, the possibility of RTS noise components will be lower, but flicker noise, I/*f* noise, in MOSFETs is generated by a superposition of RTSs caused by many individual defects [53, 123, 131], so in small dimension channel devices, the flicker noise will be lower than normal in some devices, hence, the equivalent input gate voltage noise will be lower than the prediction (Figure 9.11, dashed lines), then the number of minimum detectable charges will be lower than prediction.

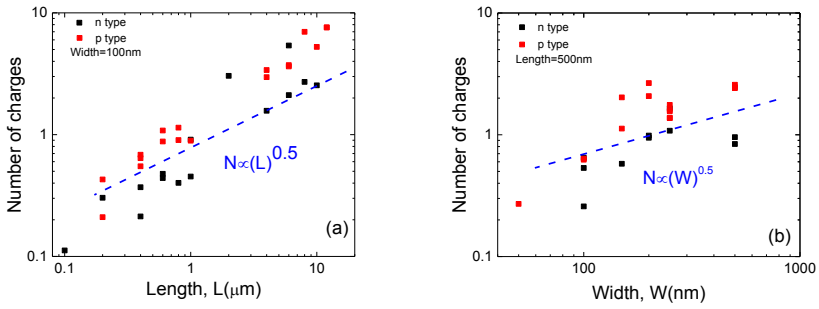


Figure 9.12 Number of minimum detectable charges estimated using noise spectra as a function of channel length (a) and width (b) of Si NW FET devices, dashed lines show a power law with exponent of 0.5, measurement error of noise spectral density is about 10%. NW length ranges from 0.1 μm to 12 μm and width ranges from 50 nm to 500 nm.

9.3 Summary

Si NW FETs with different width and length have been fabricated using a top-down fabrication technique. The Si NW FETs show stable DC characteristics and ignorable hysteresis sweeps. Low frequency noise of the Si NW FETs were measured in order to investigate the noise behavior and further evaluate the signal to noise ratio. The noise characteristics follow the correlated-mobility fluctuation model from weak inversion up to strong inversion. The operation point of the Si NW FETs should be near the region of peak transconductance because the Si NW FETs shows higher SNR in this region for long nanowire samples for p-type devices. In short nanowire samples and n-type devices, the operation point may be chosen regardless of liquid gate voltage, but in order to decrease the leakage current, it is better to choose the lower liquid gate voltage. This results indicate that the minimum detectable charge to be around 0.1 elementary charges for Si NW FETs with 0.1 μm length and 100 nm width.

Such low numbers of detectable charges are very important and open new possibilities for development of liquid gate Si NW FETs with extreme high sensitivity. In particular, RTS noise as one of the noise components appear in short channel devices, the description and analyzing are given in the next chapter.

10. RTS Noise as an Analysis Tool for High Sensitive Electrical Biosensors

Si NW FETs have attracted increased attention in the field of bioelectronics research, because they offer high sensitivity, label free and real time detection [8, 14, 23]. NW structures provide enhanced sensitivity and spatial resolution compared with conventional planar FETs, due to their higher surface to volume ratio. However, with the downscaling of the nanowre FET, the low-frequency noise is progressively becoming a serious issue [154]. Power spectrum density of drain current fluctuations in MOSFETs at low frequency follows the $1/f$ law, meaning that the noise spectrum is inversely proportional to the frequency, f, on a logarithm scale. The $1/f$ noise is generally interpreted as the superposition of random events of charge trapping and de-trapping from defects randomly distributed in the gate oxide (SiO_2) near the semiconductor channel (Si). When the critical size decreases down to the submicrometer regime, only a few traps exist, and we observe discrete switching of the drain current between two (or more) levels under constant bias conditions. These fluctuations, known as random telegraph signals (RTSs), give a Lorentzian distribution in the power spectrum density of drain current noise [155]. RTSs may decrease the signal to noise ratio (SNR), hence RTSs is a critical limit during the biosensor application.

In this chapter, the results of studying RTS noise behavior of Si NW FETs are given, measured in different pH solutions. It is revealed that there is effective modulation of the charged state of the trap by different pH solutions. The state of a single trap appears to be extremely sensitive to the number of carriers in the conducting channel. It can be considered as an analysis tool for biosensor applications.

10.1 Experimental Details

Figure 10.1 shows the SEM image of the fabricated Si NW FET devices. The design and main steps of the fabrication process can be found in Chapter 4.5 and Appendices B.4.

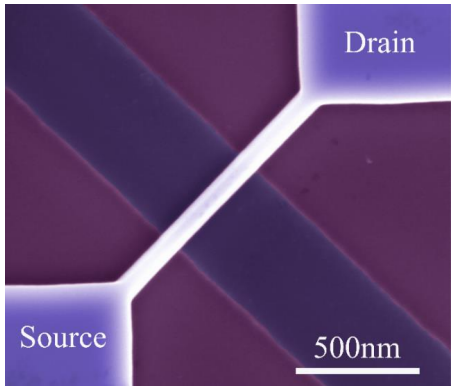


Figure 10.1 False-colored SEM image of a Si NW FET device [156].

Si NW FETs with 500 nm length and 100 nm and 200 nm width nanowires were selected for the DC and low-frequency noise characterization. The DC characteristics of the devices were measured using a semiconductor parameter analyzer (K4200, Keithely). For the initial measurement, we used 0.01 M phosphate buffered saline (PBS, Sigma-Aldrich) with pH of 7.4. To investigate the pH sensitivity of the Si NW FET, the pH value of the buffer solution was changed in the range from 5 to 8.5. A dynamic signal analyzer (HP35670A) is used for the low-frequency noise measurements in the frequency range from 1 Hz to 100 kHz. In order to avoid any influence from the environment, the pH solution was changed using a pump.

10.2 Results and Discussion

10.2.1 Electric Measurements of Fabricated Si NW FETs

Figure 10.2 shows the drain current (I_{DS}) vs. gate voltage (V_{GS}) characteristics of the Si NW FET, measured at a small drain voltage, V_{DS} = -0.1 V. During the measurement, the gate voltage was swept from -2 V to 0.5 V; the source and substrate were grounded. The Si NW FETs show typical p-type FET behavior with a high on-off value, and a subthreshold slope of 120 mV/decade.

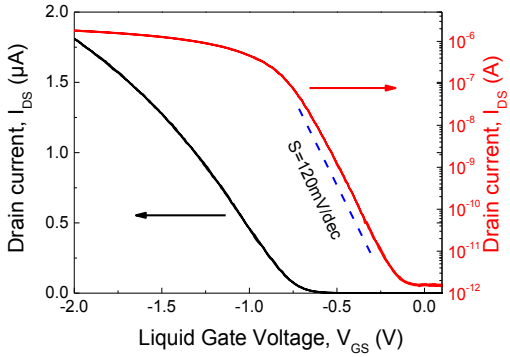


Figure 10.2 The hysteresis sweep of transfer characteristics for a Si NW FET measured at V_{DS} = -0.1 V in 10 mM PBS solution is shown in linear and logarithmic scale. The nanowire length = 0.5 μm and width = 200 nm. The subthreshold slope is close to 120 mV/dec.

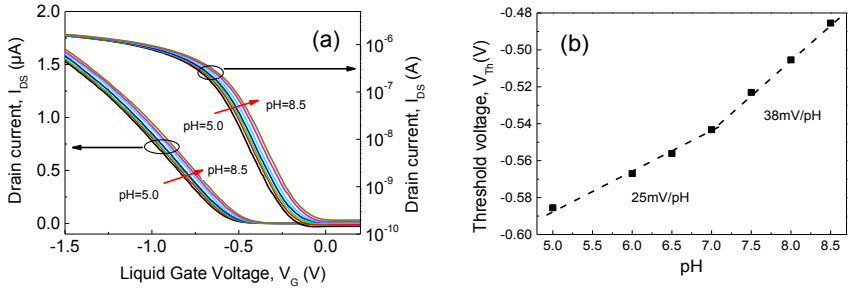


Figure 10.3 (a) Transfer characteristics of the Si NW FET measured at V_{DS} = -0.1 V at different pH values in linear and logarithmic scale. The length of the Si NW FET is 500 nm and the width is 100 nm. (b) Shift in threshold voltage (V_{Th}) with pH values, as extracted from the data shown in (a).

The transfer curves of the Si NW FET under different pH conditions are presented in Figure 10.3 (a). The transfer curve shift is correlated to the pH value. The threshold voltage (V_{Th}) of the device increases as the pH value increases as shown in Figure 10.3 (b). The pH sensitivity of the Si NW FET device is from 25 to 37mV/pH, which is a typical value [157] for FETs using a SiO_2 gate insulator as a sensing layer, without any modification.

10.2.2 Lorentzian Component Behavior in Different pH Solutions

At submicrometer feature sizes of the transistor channel, the drain current noise can be determined mainly by several traps in the gate dielectric with energy close to the Fermi level of the channel. In this case, the noise may even be observed from an individual oxide trap in the form of RTS that dominates the flicker noise. The Lorentzian components of the noise spectra are registered and their behavior allows us to analyze the trapping/detrapping processes in the gate dielectric layer.

In this work, measurements were characterized at a small drain-source voltage, V_{DS} = - 0.1 V, in order to observe the RTS noise signal. A special liquid gate voltage was chosen, V_{GS} = - 0.9 V, then the solution was changed to different pH values. At each pH solution state, the drain-source current, noise spectra, and time dependent current fluctuations were recorded.

In noise spectra, Lorentzian noise components were observed. The power spectra density of drain current noise multiplied by f, show well resolved maxima, which shift with change of pH solution as shown in Figure 10.4 (a). These curves can be well-fit by a Lorentzian function, $S(f) = S(0)/[1+(f/f_0)^2]$, where f_0 represents the characteristic frequency. The characteristic frequencies were obtained as maxima of the Lorentzian shaped components shown in Figure 10.4 (a). It should be noted that the characteristic frequency change with the value of pH solutions. When changing the value of pH solution from pH 5.5 to pH 8.5, the characteristic frequency of the Lorentzian component shifts in the noise spectra from 80 Hz to 180 Hz as shown in Figure 10.4 (b).

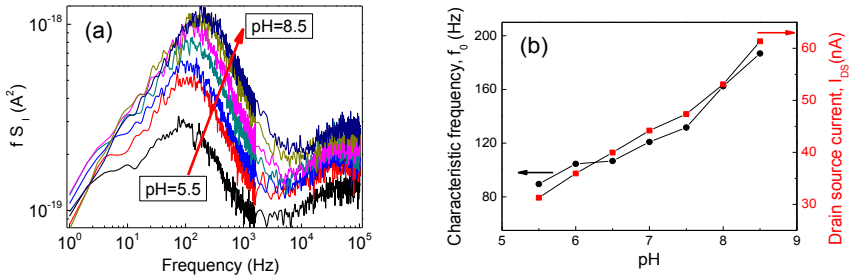
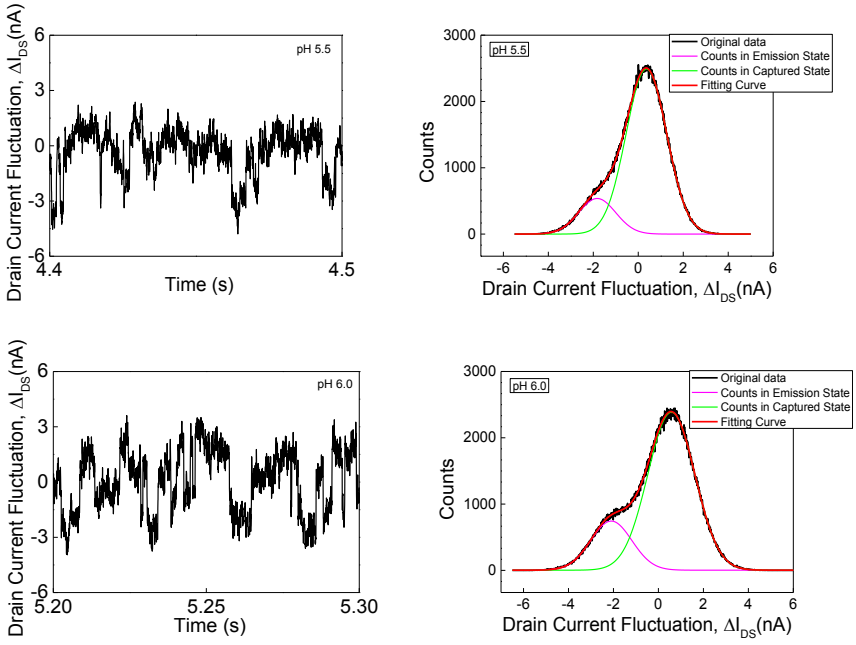


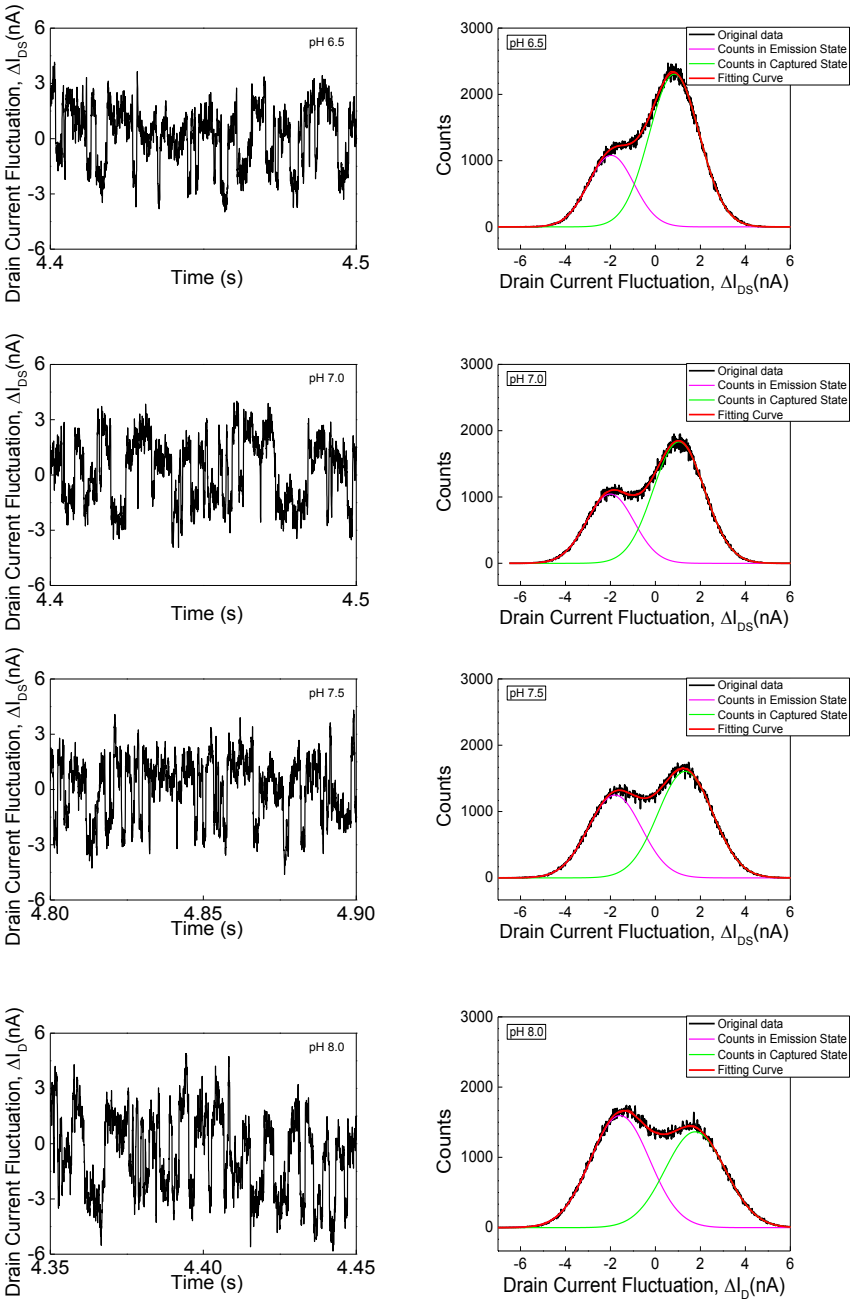
Figure 10.4 Drain current noise spectral density of Si NW FET multiplied by frequency at different pH values, measured at V_{GS} = -0.9 V, V_{DS} = -0.1 V. (b) Characteristic frequency of the Lorentzian components (data of the Figure 2 (a)) and drain current as a function of pH value.

As a pH sensor with SiO_2 as the dielectric layer, the silanol group can perform the function of a receptor for hydrogen ions in the Si NWFET. The increase in conductance indicates the

electrical gating effect changing due to debonding of hydrogen ions from the surface of dielectric layer of p-type Si NW FETs from pH = 5 to pH = 8.5. The current measured as a function of pH value is shown in Figure 10.4 (b).

Drain current fluctuations were recorded from the Si NW FET in real-time measurements (Figure 10.5 (left)) at different pH solutions. The corresponding histograms of the drain current data are plotted in Figure 10.5 (right) for more detailed analysis. For the case of two discrete levels of Drain current, at pH=5, 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 8.5, the corresponding histogram plot in Figure 10.5 (right) shows two distinct peaks with two background Gaussian distributions, indicating a single trap near the interface. The carriers are captured/decaptured to/from the trap by tunneling. At a certain bias condition, this trap in the dielectric resides in the band gap within 2*kT* of the channel Fermi level, and is within a favorable distance from the channel to be able to be electrically active in the reversible capture and emission processes with the channel carriers. The low current level corresponds to the state when one carrier is captured by trap while the high current level corresponds to the empty state.




pH 6.5
Drain Current Fluctuation, ΔI_DS(nA)
Time (s)
Original data
Counts in Emission State
Counts in Captured State
Fitting Curve
Counts
Drain Current Fluctuation, ΔI_DS(nA)
pH 7.0
pH 7.5
pH 8.0
Drain Current Fluctuation, ΔI_D(nA)

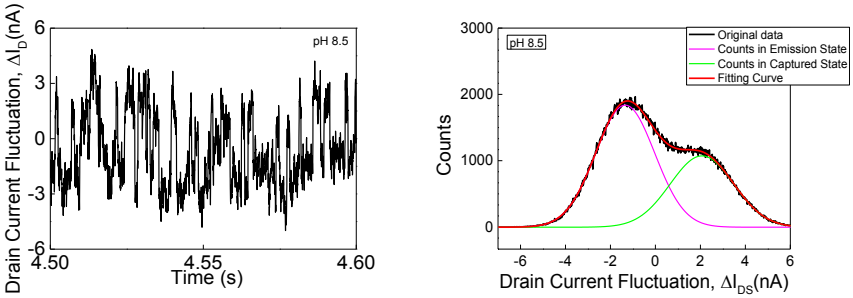


Figure 10.5 RTSs in the Si NW FET. Typical time dependence (left) and its corresponding histogram (right) of the FET drain current fluctuation, measured in solution at pH = 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 8.5.

The histogram of the RTS trace separates into two clearly resolved Gaussian peaks as seen in Figure 10.5 (right). The ratio of peak heights corresponds to the relation between capture and emission times (τ_c and τ_e, respectively), because the height of each peak is related to the time that the system spends in each state. The distance between the peaks equals the RTS amplitude, ΔV_{DS}. The time constant τ of the Lorentzian component in the noise spectra related to RTS noise can be expressed:

$$\tau = \frac{1}{2\pi f_0} \tag{9.6}$$

$$\tau = \frac{\tau_c \tau_e}{\tau_c + \tau_e} \tag{9.7}$$

Using the value of τ obtained from the spectra, and the τ_c/τ_e relation obtained from the histogram, the values of τ_c and τ_e can be obtained as shown in Figure 10.6.

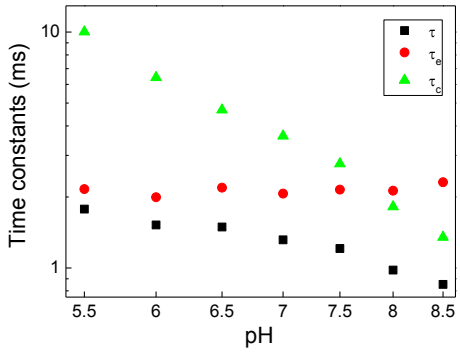


Figure 10.6 Capture (τ_c) and emission (τ_e) time constants and characteristic time constant (τ) of the RTS noise plotted as a function of different pH extracted from the histogram in Figure 10.5 at V_{DS} = - 100 mV, V_{GS} = - 0.9 V.

Comparing Figure 10.6 and Figure 10.4 (a), we can calculate the sensitivity of the time dependence measurement and frequency measurement as shown in Figure 10.7. It demonstrates that the capture time calculated from the frequency domain measurements has a higher sensitivity than conventional technique based on the tracking of drain current changes.

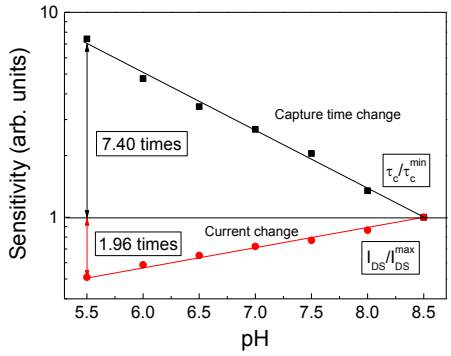


Figure 10.7 Sensitivity extracted from the pH dependence of the drain current and RTS capture time constant.

Analysis of the results dynamic characteristics of the active centers in semiconductors is usually performed with in the frame work of the Shockley Read Hall (SRH) model [129, 130], according to which:

$$\tau_c = \frac{1}{\sigma_p v_{th} p} \tag{9.8}$$

$$\tau_e = \frac{1}{\sigma_p v_{th} p_1} = \frac{1}{\sigma_p v_{th} N_v} exp\left(\frac{E_b}{kT}\right) \tag{9.9}$$

where σ_p is the capture cross section, v_{th} is the average thermal velocity, p is the concentration of free holes (in the case of hole capture), p_1 is the statistical factor v-band, N_v is the effective density of states in the valence band, and E_b is the energy level of the center with respect to the top of the valence band.

According to Equation (9.8), at a certain temperature *T*, the capture time τ_c is inversely proportional to the concentration of free holes *p*. In our case, we can use the fact that this value determines the amount of current through the channel. If the mobility dependence on the gate voltage can be neglected, then the applicability of the model SRH can be proved by plotting $\tau_c = f(I_{DS})$.

In linear operation, where in the accumulation layer's surface density of p is proportional to the drain current I_{DS}. According to the SRH model, τ_c is inversely proportional to the drain current I_{DS} in linear operation.

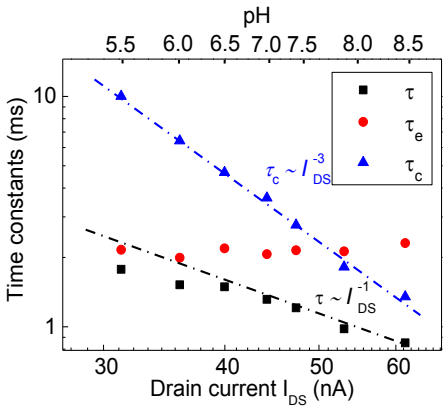


Figure 10.8 Capture (τ_c) and emission (τ_e) time constants and characteristic time constant (τ) of the RTS noise plotted as a function of different pH and drain currents at V_{DS} = -100 mV, V_{GS} = -0.9 V. Points are connected with lines as a guide to the eye. Dashed lines indicate different behaviors with slopes: (-3) for our experimental data, (-1) for the conventional Shockley-Read-Hall model.

However, from Figure 10.8, the dependence of τ_C on current is $\tau_c \propto I_{DS}^{-3}$. Such a behavior does not correspond to Schockley-Read-Hall theory ($\tau_c \propto I_{DS}^{-1}$). Such anomalous dependence on current can be explained by introducing the concept of Coulomb blockade Energy, which is necessary for an electron (or hole) to overcome, while moving from the channel to the trap in the dielectric layer [56, 123]. So Equation (9.8) can be rewritten as:

$$\tau_c = \frac{1}{\sigma_p v_{th} p} \exp\left(\frac{\Delta E}{kT}\right) \tag{9.10}$$

Where ΔE is Coulomb blockade energy. As we can see from Figure 10.8, τ_e does not depend on current, and thus we can assume that σ_p in Equation (9.16) and Equation (9.9) are the same. If we neglect the difference of the hole velocity, v_{th}, then the deviation between our case the SRH theory is because of the Coulomb blockade energy ΔE, which is inversely proportional to the logarithm of the carrier density .

It should be emphasized that the current I_{DS} here is proportional to the concentration of free holes at the interface. However, the concentration of free holes is in dependence on the pH value, as is revealed in Figure 10.4 (a). Therefore, the Coulomb blockade energy ΔE is dependent on the pH value, and further the capture time τ_C depends on the pH value.

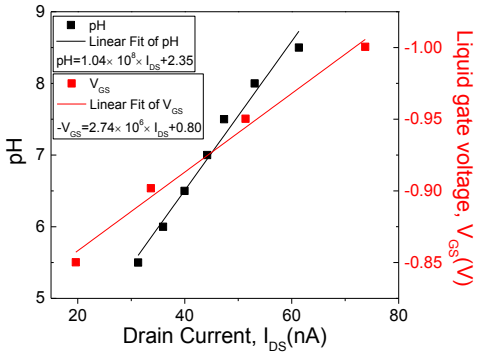


Figure 10.9 Relation of pH value (black curve) and gate voltage (red curve) with drain current

We assume that drain current is related to pH and drain current depend on the gate voltage. Figure 10.9 demonstrates the pH value and gate voltage as a function of drain current. The pH dependent drain current was obtained from the measurements with a stable working point, V_{GS} = - 0.9 V, by changing the pH of the solution to a different value. The current dependence of the gate voltage was obtained from the gate voltage dependent measurements. During the measurements, PBS solution was used as the electrolyte environment with a constant pH value of 7.4. The linear fitting data give us the following relations:

$$pH = 1.04 \times 10^8 \times I_{DS} + 2.346 \tag{9.11}$$

$$-V_{GS} = 2.74 \times 10^6 \times I_{DS} + 0.80335 \tag{9.12}$$

From the two equations above, we can get: $\Delta V_{Th}/\Delta pH$ = 26.35 mV/pH, which coincides with our measurement results (see Figure 10.3 (b)).

10.3 Summary

In summary, random telegraph signals are observed in Si NW field effect transistors, and Lorentzian components were recorded in different pH solutions. The data demonstrate that the capture time extracted from the Lorentzian component is as a function of pH value of different solutions. Our results show that the frequency domain analysis is more sensitive than conventional technique based on the tracking of drain current changes. Therefore, it provides a powerful method complementary to the real-time detection, and should be especially useful for biosensor analysis.

11. Conclusion and Outlook

11.1 Conclusion

In this thesis, the "top down" approach combining the NIL and EBL with TMAH chemical etching techniques were used to fabricate Si NW FET biosensors with reproducible results.

T-NIL was employed for fabrication of the Si NW chips due to their low cost, high throughput and high-resolution properties. The design and fabrication of the nanoimprint mold is very critical during the NIL. The resolution is limited by the features' sizes of the fabricated mold. In this work, we fabricated a high-quality nanoimprint mold, during this process, KOH chemical etching was used for the first time for the mold fabrication. The mold is based on a Si <110> wafer with structures down to 50 nm resolution and vertical side walls obtained due to anisotropical chemical etching. The design and imprint conditions (pressure, temperature, and spin speed) were optimized and lead to a uniform distribution of the resist, under the optimized conditions, it can fabricate the Si NW FET devices with 100% yield and high resolution.

TMAH etching was used to transfer the structures of both contact lines and NWs defined by NIL to the SOI wafer. As TMAH is an anisotropic etching technique, the etching rate of the <111> face is much slower than the other faces. Therefore after chemical etching trapezoid shape cross-section of the NWs were formed, the smallest size was tens of nanometers.

During my PhD work, four kinds of devices were fabricated based on the above technologies.

- Back gate Si NW FETs with micrometer channels.
- Back gate Si NW FETs with submicrometer channels.
- Si NW FET biosensors fabricated by T-NIL with micrometer channels.
- Si NW FET biosensors fabricated by EBL with submicrometer channels.

The Si NW FETs were characterized by I_{DS}-V_G characteristics and low-frequency noise spectra measurements at different backgate voltages in ambient conditions and different front gate voltages with a liquid gate. RTS components were registered in short channel FETs for both backgate and front gate configurations.

The results of electrical measurements for the samples with different channel length show that the contact resistance is one order of magnitude smaller than the total resistance. Trap density, estimated from flicker noise, was found to be about $5 \times 10^{17} cm^{-3}$, which is of the order of magnitude of good quality bulk silicon material. The samples demonstrate high-mobility, 750 cm^2/Vs, and low-noise due to the improved technology and TMAH chemical etching.

Transport properties of p-type Si NW FETs with a cross-section of 42 x 42 nm^2 were studied utilizing noise spectroscopy. The values of volume trap density obtained from the level of

input voltage spectral density are much lower than those obtained for conventional CMOS devices. The devices with different channel lengths have almost the same input voltage spectral density, indicating that the influence of contact effects on the performance of the investigated devices can be neglected. Analysis of the registered RTS noise component reveals that a single trap is located near one of the ohmic contacts in the gate dielectric. Estimated parameters of the trap and its behavior demonstrate that even a single carrier process in the gate of the NW transistor considerably modulates current in the channel. These results are promising for advanced control of the channel transport in NW FETs, including the possibility of single molecule detection with increased sensitivity using the modulation effect of the channel conductivity in Si NW FET.

Sub-µm size backgate FETs were fabricated using novel NIL combined with the TMAH etching technique. RTSs at different temperatures from 200 K to 280 K were registered in such a device. The Coulomb energy involved during trapping and detrapping of an elementary charge in an interface trap was studied. The results exhibit a deviation of the single interface trap behavior from the classical Shockley-Read-Hall laws. The difference can predominantly be explained by accounting for the Coulomb energy, which is linearly proportional to temperature and decreases logarithmically with inversion carrier density in the channel due to screening.

High quality Si NW FET biosensors with different width and length have been fabricated using a top-down NIL silicon fabrication technique. It shows stable DC characteristics and the pH sensitivity of the device is 33 mV/pH and 41 mV/pH without with APTES modification and, respectively. Low frequency noise of the Si NW FET was measured to investigate the noise behavior and the minimum charges detectable with our devices. These results indicate that the number of detectable minimum charges on the Si NW FET sensor increases proportionally with the square root of channel surface area. This scaling rule gives us the prospect of designing and fabricating biosensors for single molecule detection applications.

In order to detect single charged molecules and study the RTSs in submicron dimension Si NW FETs, with different width and length, have been fabricated using a top-down silicon fabrication technique with EBL. The Si NW biosensors show, for both p and n-type FETs, stable DC characteristics and the pH sensitivity of the devices is more than 25 mV/pH. Low frequency noise of the Si NW biosensors were measured to investigate the noise behavior and signal to noise ratio. The results indicated an obvious difference in input referred gate noise for the two types of devices. In the case of n-type Si NW FETs, the input referred gate noise was always independent of liquid gate voltage. However, in the case of p-type Si NW FETs, the input referred gate noise was only liquid gate dependent in long (>1 µm) Si NW FETs. These FETs have a minimum referred input gate noise near the maximum transconductance conditions. The number of detectable minimum charges was calculated from the obtained results, these results coincide with the trend shown in devices of the last paragraph and indicate that the minimum detectable charge is around 0.1 elementary charge for our bio-FETs with 0.1 µm length and 100 nm width. The short channel effect was additionally observed when the channel is smaller than 1 µm. However, this effect can be effectively eliminated by decreasing the channel dimensions. When NW width was reduced to 200 nm or less, the short

channel effects in low length FETs was reduced. This increases the stability of V_{Th} in the small FETs.

Random telegraph signals were also observed in the Si NW field effect transistors with submicron channels. Lorentzian components were recorded in different pH solutions. The data demonstrates that the capture time extracted from the Lorentzian component is a function of the pH value of different solutions. Our results show that the frequency domain analysis is more sensitive than drain current over time trace measurements alone. The reason can be explained by the consideration of Coulomb Blockade energy. Therefore, RTS analysis provides a powerful method complementary to the real-time current detection, and should be especially useful for biosensor analysis.

11.2 Outlook

As described above, the fabrication process for the Si NW FET structures were established. However, the devices still need to be improved in order to be used for industry applications. Several possible improvements are discussed here.

The microfluidic approach should be taken into account, since it allows the exchange of the solutions in a much more convenient way than simple exchange of the electrolyte in the bath. Integrating the reference electrode with the nanowire device is attractive as it can let the device work with the microfluidics and decrease the price.

In order to study the single charge or signal from single biomolecules, the nanowire channel should be minimized until it is possible to reach such a target. RTS noise also can be expected for use as a method for increasing the sensitivity of biosensors.

Specific chemical or biological molecules that can influence the surface potential of the NW can be detected using the biosensor with the single charge detectability. With respect to strengthening the modulation effect from the single molecule binding activities, it will be interesting to study the influence of the screening effect in the electrolyte using RTSs from the binding and debinding of biomolecules.

Another useful application is the detection of cell activity, including the action potential of a single neuron. It also is a promising method to study the communication between neurons by means of mapping living neuronal networks using arrays of NW FETs.

Thus, the work presented in this thesis may provide a new platform for the fabrication and characterization of Si NW FET devices, which are useful for a large number of biosensor applications. Label-free FET biosensors with an integrated transducer, developed on the basis of electronic read out, may greatly decrease costs and offer and exciting prospect in clinical, basic research, and public health applications, including home-available portable medical care systems.

References

[1] W. F. Brinkman, D. E. Haggan, and W. W. Troutman, "A history of the invention of the transistor and where it will lead us," *Ieee Journal of Solid-State Circuits,* vol. 32, pp. 1858-1865, Dec 1997.

[2] K. Dawon, "Electric field controlled semiconductor device," US Patent, 1963.

[3] G. E. Moore, "Cramming more components onto integrated circuits (Reprinted from Electronics, pg 114-117, April 19, 1965)," *Proceedings of the Ieee,* vol. 86, pp. 82-85, Jan 1998.

[4] F. Patolsky and C. M. Lieber, "Nanowire nanosensors," *Materials Today,* vol. 8, pp. 20-28, 2005.

[5] J. Wang, "Nanomaterial-based electrochemical biosensors," *Analyst,* vol. 130, pp. 421-426, 2005.

[6] F.-G. Banica, *Chemical sensors and biosensors : fundamentals and applications*. Chichester, West Sussex, United Kingdom: John Wiley & Sons Inc., 2012.

[7] A. M. Morales and C. M. Lieber, "A laser ablation method for the synthesis of crystalline semiconductor nanowires," *Science,* vol. 279, pp. 208-11, Jan 9 1998.

[8] Y. Cui, Q. Q. Wei, H. K. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science,* vol. 293, pp. 1289-1292, Aug 17 2001.

[9] R. J. Chen, S. Bangsaruntip, K. A. Drouvalakis, N. W. S. Kam, M. Shim, Y. M. Li*, et al.*, "Noncovalent functionalization of carbon nanotubes for highly specific electronic biosensors," *Proceedings of the National Academy of Sciences of the United States of America,* vol. 100, pp. 4984-4989, Apr 29 2003.

[10] M. Dahan, S. Levi, C. Luccardini, P. Rostaing, B. Riveau, and A. Triller, "Diffusion dynamics of glycine receptors revealed by single-quantum dot tracking," *Science,* vol. 302, pp. 442-445, Oct 17 2003.

[11] N. S. Ramgir, Y. Yang, and M. Zacharias, "Nanowire-Based Sensors," *Small,* vol. 6, pp. 1705-1722, Aug 2010.

[12] F. Patolsky, G. Zheng, and C. M. Lieber, "Nanowire sensors for medicine and the life sciences," *Nanomedicine,* vol. 1, pp. 51-65, Jun 2006.

[13] G. F. Zheng, F. Patolsky, Y. Cui, W. U. Wang, and C. M. Lieber, "Multiplexed electrical detection of cancer markers with nanowire sensor arrays," *Nature Biotechnology,* vol. 23, pp. 1294-1301, Oct 2005.

[14] X. X. Duan, Y. Li, N. K. Rajan, D. A. Routenberg, Y. Modis, and M. A. Reed, "Quantification of the affinities and kinetics of protein interactions using silicon nanowire biosensors," *Nature Nanotechnology,* vol. 7, pp. 401-407, Jun 2012.

[15] J. Hahm and C. M. Lieber, "Direct ultrasensitive electrical detection of DNA and DNA sequence variations using nanowire nanosensors," *Nano Letters,* vol. 4, pp. 51-54, Jan 2004.

[16] F. Patolsky, G. F. Zheng, O. Hayden, M. Lakadamyali, X. W. Zhuang, and C. M. Lieber, "Electrical detection of single viruses," *Proceedings of the National Academy of Sciences of the United States of America,* vol. 101, pp. 14017-14022, Sep 28 2004.

[17] X. J. Duan, R. X. Gao, P. Xie, T. Cohen-Karni, Q. Qing, H. S. Choe*, et al.*, "Intracellular recordings of action potentials by an extracellular nanoscale field-effect transistor," *Nature Nanotechnology,* vol. 7, pp. 174-179, Mar 2012.

[18] Q. Qing, S. K. Pal, B. Tian, X. Duan, B. P. Timko, T. Cohen-Karni*, et al.*, "Nanowire transistor arrays for mapping neural circuits in acute brain slices," *Proc Natl Acad Sci U S A,* vol. 107, pp. 1882-7, Feb 2 2010.

[19] B. P. Timko, F. Patolsky, and C. M. Lieber, "Response to Comment on "Detection, Stimulation, and Inhibition of Neuronal Signals with High-Density Nanowire Transistor Arrays"," *Science,* vol. 323, Mar 13 2009.

[20] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, 3rd ed. New Dehli: Wiley-India, 2007.

[21] R. G. Hobbs, N. Petkov, and J. D. Holmes, "Semiconductor Nanowire Fabrication by Bottom-Up and Top-Down Paradigms," *Chemistry of Materials,* vol. 24, pp. 1975-1991, Jun 12 2012.

[22] M. W. Li, R. B. Bhiladvala, T. J. Morrow, J. A. Sioss, K. K. Lew, J. M. Redwing*, et al.*, "Bottom-up assembly of large-area nanowire resonator arrays," *Nature Nanotechnology,* vol. 3, pp. 88-92, Feb 2008.

[23] E. Stern, J. F. Klemic, D. A. Routenberg, P. N. Wyrembak, D. B. Turner-Evans, A. D. Hamilton*, et al.*, "Label-free immunodetection with CMOS-compatible semiconducting nanowires," *Nature,* vol. 445, pp. 519-522, Feb 1 2007.

[24] E. Stern, A. Vacic, and M. A. Reed, "Semiconducting Nanowire Field-Effect Transistor Biomolecular Sensors," *Ieee Transactions on Electron Devices,* vol. 55, pp. 3119-3130, Nov 2008.

[25] F. N. Hooge, "1/f noise sources," *Electron Devices, IEEE Transactions on,* vol. 41, pp. 1926-1935, 1994.

[26] N. K. Rajan, D. A. Routenberg, J. Chen, and M. A. Reed, "1/f Noise of Silicon Nanowire BioFETs," *Ieee Electron Device Letters,* vol. 31, pp. 615-617, Jun 2010.

[27] N. K. Rajan, D. A. Routenberg, and M. A. Reed, "Optimal signal-to-noise ratio for silicon nanowire biochemical sensors," *Applied Physics Letters,* vol. 98, Jun 27 2011.

[28] A. Tarasov, W. Fu, O. Knopfmacher, J. Brunner, M. Calame, and C. Schonenberger, "Signal-to-noise ratio in dual-gated silicon nanoribbon field-effect sensors," *Applied Physics Letters,* vol. 98, Jan 3 2011.

[29] L. K. J. Vandamme, X. S. Li, and D. Rigaud, "1/F Noise in Mos Devices, Mobility or Number Fluctuations," *Ieee Transactions on Electron Devices,* vol. 41, pp. 1936-1945, Nov 1994.

[30] P. Bergveld, "Development, Operation, and Application of the Ion-Sensitive Field-Effect Transistor as a Tool for Electrophysiology," *Ieee Transactions on Biomedical Engineering,* vol. BM19, pp. 342-&, 1972 1972.

[31] X. T. Vu, "Silicon nanowire transistor arrays for biomolecular detection," PhD, RWTH Aachen, 2011.

[32] P. Bergveld, "Thirty years of ISFETOLOGY - What happened in the past 30 years and what may happen in the next 30 years," *Sensors and Actuators B-Chemical,* vol. 88, pp. 1-20, Jan 1 2003.

[33] X. R. Yang, W. R. Frensley, D. Zhou, and W. C. Hu, "Performance Analysis of Si Nanowire Biosensor by Numerical Modeling for Charge Sensing," *Ieee Transactions on Nanotechnology,* vol. 11, pp. 501-512, May 2012.

[34] S. Y. Chen, J. G. Bomer, E. T. Carlen, and A. van den Berg, "Al2O3/Silicon NanoISFET with Near Ideal Nernstian Response," *Nano Letters,* vol. 11, pp. 2334-2341, Jun 2011.

[35] E. McCafferty and J. P. Wightman, "Determination of the concentration of surface hydroxyl groups on metal oxide films by a quantitative XPS method," *Surface and Interface Analysis,* vol. 26, pp. 549-564, Jul 1998.

[36] D. E. Yates, S. Levine, and T. W. Healy, "Site-binding model of the electrical double layer at the oxide/water interface," *Journal of the Chemical Society, Faraday Transactions 1: Physical Chemistry in Condensed Phases,* vol. 70, pp. 1807-1818, 1974.

[37] T. W. Healy and L. R. White, "Ionizable surface group models of aqueous interfaces," *Advances in Colloid and Interface Science,* vol. 9, pp. 303-345, 6// 1978.

[38] L. Bousse, N. F. De Rooij, and P. Bergveld, "Operation of chemically sensitive field-effect sensors as a function of the insulator-electrolyte interface," *Electron Devices, IEEE Transactions on,* vol. 30, pp. 1263-1270, 1983.

[39] A. van den Berg, P. Bergveld, D. N. Reinhoudt, and E. J. Sudhölter, "Sensitivity control of ISFETs by chemical surface modification," *Sensors and Actuators,* vol. 8, pp. 129-148, 10// 1985.

[40] R. E. G. van Hal, J. C. T. Eijkel, and P. Bergveld, "A general model to describe the electrostatic potential at electrolyte oxide interfaces," *Advances in Colloid and Interface Science,* vol. 69, pp. 31-62, 12/1/ 1996.

[41] Y. Cui and C. M. Lieber, "Functional nanoscale electronic devices assembled using silicon nanowire building blocks," *Science,* vol. 291, pp. 851-3, Feb 2 2001.

[42] Y. Cui, Z. H. Zhong, D. L. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Letters,* vol. 3, pp. 149-152, Feb 2003.

[43] T. Cohen-Karni and C. M. Lieber, "Nanowire nanoelectronics: Building interfaces with tissue and cells at the natural scale of biology," *Pure and Applied Chemistry,* vol. 85, pp. 883-901, 2013.

[44] E. Stern, R. Wagner, F. J. Sigworth, R. Breaker, T. M. Fahmy, and M. A. Reed, "Importance of the debye screening length on nanowire field effect transistor sensors," *Nano Letters,* vol. 7, pp. 3405-3409, 2007.

[45] S. Baumgartner, C. Heitzinger, A. Vacic, and M. A. Reed, "Predictive simulations and optimization of nanowire field-effect PSA sensors including screening," *Nanotechnology,* vol. 24, p. 225503, Jun 7 2013.

[46] K. I. Chen, B. R. Li, and Y. T. Chen, "Silicon nanowire field-effect transistor-based biosensors for biomedical diagnosis and cellular recording investigation," *Nano Today,* vol. 6, pp. 131-154, Apr 2011.

[47] G. J. Zhang and Y. Ning, "Silicon nanowire biosensor and its applications in disease diagnostics: A review," *Analytica Chimica Acta,* vol. 749, pp. 1-15, Oct 2012.

[48] Y. X. Liu, K. Ishii, T. Tsutsumi, M. Masahara, and E. Suzuki, "Ideal rectangular cross-section Si-Fin channel double-gate MOSFETs fabricated using orientation-dependent wet etching," *Ieee Electron Device Letters,* vol. 24, pp. 484-486, Jul 2003.

[49] G. F. Zheng, F. Patolsky, and C. M. Lieber, "Large-scale, multiplexed electrical detection of proteins and viruses by ultrasensitive nanowire sensor arrays," *Abstracts of Papers of the American Chemical Society,* vol. 230, pp. U306-U307, Aug 28 2005.

[50] M. Von Haartman and M. Östling, *Low-frequency noise in advanced MOS devices*. Dordrecht: Springer, 2007.

[51] C. D. Motchenbacher, J. A. Connelly, D. C. Fitchen, and C. D. Motchenbacher, *Low-noise electronic system design*. New York ; Chichester: Wiley, 1993.

[52] W. Schottky, "Über spontane Stromschwankungen in verschiedenen Elektrizitätsleitern," *Annalen der Physik,* vol. 362, pp. 541-567, 1918.

[53] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/ƒ) noise," *Advances in Physics,* vol. 38, pp. 367-468, Jul-Aug 1989.

[54] K. Kandiah, M. O. Deighton, and F. B. Whiting, "A physical model for random telegraph signal currents in semiconductor devices," *Journal of Applied Physics,* vol. 66, pp. 937-948, Jul 15 1989.

[55] T. G. M. Kleinpenning, "On 1/f noise and random telegraph noise in very small electronic devices," *Physica B,* vol. 164, pp. 331-334, Sep 1990.

[56] M. Schulz, "Coulomb Energy of Traps in Semiconductor Space-Charge Regions," *Journal of Applied Physics,* vol. 74, pp. 2649-2657, Aug 15 1993.

[57] L. K. J. Vandamme, "On the origin of 1/f noise in mosfets," *Fluctuation and Noise Letters,* vol. 7, pp. L321-L339, Sep 2007.

[58] G. Ghibaudo, O. Roux, C. Nguyenduc, F. Balestra, and J. Brini, "Improved Analysis of Low Frequency Noise in Field-Effect MOS Transistors," *Physica Status Solidi a-Applied Research,* vol. 124, pp. 571-581, Apr 16 1991.

[59] I. M. Hafez, G. Ghibaudo, and F. Balestra, "A study of flicker noise in MOS transistors operated in the linear and non linear regions at room and liquid helium temperatures " *Solid-State Electronics,* vol. 33, pp. 1525-1529, Dec 1990.

[60] F. N. Hooge, "1-F Noise," *Physica B & C,* vol. 83, pp. 14-23, 1976.

[61] A. A. Tseng, C. Kuan, C. D. Chen, and K. J. Ma, "Electron beam lithography in nanoscale fabrication: recent development," *Electronics Packaging Manufacturing, IEEE Transactions on,* vol. 26, pp. 141-149, 2003.

[62] B. Q. Wu, A. Kumar, and S. Pamarthy, "High aspect ratio silicon etch: A review," *Journal of Applied Physics,* vol. 108, Sep 2010.

[63] D. Bratton, D. Yang, J. Y. Dai, and C. K. Ober, "Recent progress in high resolution lithography," *Polymers for Advanced Technologies,* vol. 17, pp. 94-103, Feb 2006.

[64] V. R. Manfrinato, L. Zhang, D. Su, H. Duan, R. G. Hobbs, E. A. Stach*, et al.*, "Resolution Limits of Electron-Beam Lithography toward the Atomic Scale," *Nano Letters,* vol. 13, pp. 1555-1558, 2013/04/10 2013.

[65] H. Sewell, A. Chen, J. Finders, and M. Dusa, "Progress in Extending Immersion Lithography for the 32 nm Node and Beyond," *Japanese Journal of Applied Physics,* vol. 48, Jun 2009.

[66] J. Joo, B. Y. Chow, and J. M. Jacobson, "Nanoscale patterning on insulating substrates by critical energy electron beam lithography," *Nano Letters,* vol. 6, pp. 2021-2025, Sep 13 2006.

[67] H. Schift, "Nanoimprint lithography: An old story in modern times? A review," *Journal of Vacuum Science & Technology B,* vol. 26, pp. 458-480, Mar-Apr 2008.

[68] S. H. Kim, K. D. Lee, J. Y. Kim, M. K. Kwon, and S. J. Park, "Fabrication of photonic crystal structures on light emitting diodes by nanoimprint lithography," *Nanotechnology,* vol. 18, Feb 7 2007.

[69] W. Wu, J. Gu, H. X. Ge, C. Keimel, and S. Y. Chou, "Room-temperature Si single-electron memory fabricated by nanoimprint lithography," *Applied Physics Letters,* vol. 83, pp. 2268-2270, Sep 15 2003.

[70] X. G. Liang, K. J. Morton, R. H. Austin, and S. Y. Chou, "Single sub-20 nm wide, centimeter-long nanofluidic channel fabricated by novel nanoimprint Mold fabrication and direct imprinting," *Nano Letters,* vol. 7, pp. 3774-3780, Dec 2007.

[71] M. Malloy and L. C. Litt, "Technology review and assessment of nanoimprint lithography for semiconductor and patterned media manufacturing," *Journal of Micro-Nanolithography Mems and Moems,* vol. 10, Jul-Sep 2011.

[72] L. J. Guo, "Nanoimprint lithography: Methods and material requirements," *Advanced Materials,* vol. 19, pp. 495-513, Feb 19 2007.

[73] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Imprint of Sub-25 Nm Vias and Trenches in Polymers," *Applied Physics Letters,* vol. 67, pp. 3114-3116, Nov 20 1995.

[74] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Imprint lithography with 25-nanometer resolution," *Science,* vol. 272, pp. 85-87, Apr 5 1996.

[75] J. Haisma, M. Verheijen, K. van den Heuvel, and J. Van den Berg, "Mold-assisted nanolithography: A process for reliable pattern replication," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 14, pp. 4124-4128, 1996.

[76] O. Tabata, "Anisotropic etching of silicon in TMAH solutions," *Sensors and Materials,* vol. 13, pp. 271-283, 2001.

[77] V. Sydoruk, "Low-frequency noise and transport characteristics of nanostructures," doctor, TU Dortmund, 2011.

[78] J. Li, S. Pud, D. Mayer, and S. Vitusevich, "Advanced fabrication of Si nanowire FET structures by means of a parallel approach," *Nanotechnology,* vol. 25, Jul 11 2014.

[79] R. B. Salazar, S. R. Mehrotra, G. Klimeck, N. Singh, and J. Appenzeller, "Observation of 1D behavior in Si nanowires: Toward high-performance TFETs," *Nano Letters,* vol. 12, pp. 5571-5575, 2012.

[80] C. S. Li, M. Bescond, and M. Lannoo, "Influence of the interface-induced electron self-energy on the subthreshold characteristics of silicon gate-all-around nanowire transistors," *Applied Physics Letters,* vol. 97, Dec 20 2010.

[81] H. K. Lim and J. G. Fossum, "Threshold Voltage of Thin-Film Silicon-on-Insulator (Soi) Mosfets," *Ieee Transactions on Electron Devices,* vol. 30, pp. 1244-1251, 1983.

[82] N. Lukyanchikova, N. Garbar, A. Smolanka, M. Lokshin, E. Simoen, and C. Claeys, "Origin of the front-back-gate coupling in partially depleted and fully depleted silicon-on-insulator metal-oxide-semiconductor field-effect transistors with accumulated back gate," *Journal of Applied Physics,* vol. 98, Dec 1 2005.

[83] R. Rurali, "Colloquium: Structural, electronic, and transport properties of silicon nanowires," *Reviews of Modern Physics,* vol. 82, pp. 427-449, Jan-Mar 2010.

[84] B. P. Timko, T. Cohen-Karni, Q. Qing, B. Z. Tian, and C. M. Lieber, "Design and Implementation of Functional Nanoelectronic Interfaces With Biomolecules, Cells, and Tissue Using Nanowire Device Arrays," *Ieee Transactions on Nanotechnology,* vol. 9, pp. 269-280, May 2010.

[85] G. F. Zheng, W. Lu, S. Jin, and C. M. Lieber, "Synthesis and fabrication of high-performance n-type silicon nanowire transistors," *Advanced Materials,* vol. 16, pp. 1890-+, Nov 4 2004.

[86] S. M. Koo, A. Fujiwara, J. P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich, "High inversion current in silicon nanowire field effect transistors," *Nano Letters,* vol. 4, pp. 2197-2201, Nov 2004.

[87] P. E. Allain, X. Le Roux, F. Parrain, and A. Bosseboeuf, "Large initial compressive stress in top-down fabricated silicon nanowires evidenced by static buckling," *Journal of Micromechanics and Microengineering,* vol. 23, Jan 2013.

[88] G. Stan, S. Krylyuk, A. V. Davydov, and R. F. Cook, "Compressive Stress Effect on the Radial Elastic Modulus of Oxidized Si Nanowires," *Nano Letters,* vol. 10, pp. 2031-2037, 2010/06/09 2010.

[89] T. Takeuchi, K. Tatsumura, T. Shimura, and I. Ohdomari, "X-ray diffraction study of strain distribution in oxidized Si nanowires," *Journal of Applied Physics,* vol. 106, Oct 1 2009.

[90] G. F. Jiao, Z. X. Chen, H. Y. Yu, X. Y. Huang, D. M. Huang, N. Singh*, et al.*, "Experimental Studies of Reliability Issues in Tunneling Field-Effect Transistors," *Ieee Electron Device Letters,* vol. 31, pp. 396-398, May 2010.

[91] T. Kasakawa, H. Tabata, R. Onodera, H. Kojima, M. Kimura, H. Hara*, et al.*, "An Artificial Neural Network at Device Level Using Simplified Architecture and Thin-Film Transistors," *Ieee Transactions on Electron Devices,* vol. 57, pp. 2744-2750, Oct 2010.

[92] M. Hu and T. Tsuchiya, "Channel Length and Time Dependent Interface Trap Generation near the Source Due to Hot-Carrier Injection in Metal-Oxide-

Semiconductor Field-Effect Transistors," *Japanese Journal of Applied Physics,* vol. 51, Jul 2012.

[93] A. Motayed, J. E. Bonevich, S. Krylyuk, A. V. Davydov, G. Aluri, and M. V. Rao, "Correlation between the performance and microstructure of Ti/Al/Ti/Au ohmic contacts to p-type silicon nanowires," *Nanotechnology,* vol. 22, 2011.

[94] Y. Huang, X. F. Duan, Y. Cui, and C. M. Lieber, "Gallium nitride nanowire nanodevices," *Nano Letters,* vol. 2, pp. 101-104, Feb 2002.

[95] A. L. McWhorter, *"1/f noise and germanium surface properties,". In Semiconductor Surface Physics*: Kingston, R. H., Ed.; University of Pennsylvania: Philadelphia, PA, 1957.

[96] G. G. Shahidi, "SOI technology for the GHz era," *Ibm Journal of Research and Development,* vol. 46, pp. 121-131, Mar-May 2002.

[97] J. Jomaah, M. Fadlallah, and G. Ghibaudo, "Low Frequency Noise Analysis in Advanced CMOS Devices," in *Advances in Innovative Materials and Applications*. vol. 324, M. Soueidan, M. Roumie, and P. Masri, Eds., ed, 2011, pp. 441-444.

[98] F. N. Hooge, "1/F Noise Is No Surface Effect," *Physics Letters A,* vol. A 29, pp. 139-&, 1969.

[99] K. Heo, E. Cho, J. E. Yang, M. H. Kim, M. Lee, B. Y. Lee*, et al.*, "Large-Scale Assembly of Silicon Nanowire Network-Based Devices Using Conventional Microfabrication Facilities," *Nano Letters,* vol. 8, pp. 4523-4527, Dec 2008.

[100] W. Lu, P. Xie, and C. M. Lieber, "Nanowire Transistor Performance Limits and Applications," *Ieee Transactions on Electron Devices,* vol. 55, pp. 2859-2876, Nov 2008.

[101] H. S. Song and T. H. Park, "Integration of biomolecules and nanomaterials: Towards highly selective and sensitive biosensors," *Biotechnology Journal,* vol. 6, pp. 1310-1316, Nov 2011.

[102] X. Liu, Y.-Z. Long, L. Liao, X. Duan, and Z. Fan, "Large-Scale Integration of Semiconductor Nanowires for High-Performance Flexible Electronics," *Acs Nano,* vol. 6, pp. 1888-1900, Mar 2012.

[103] T. Kong, R. Su, B. Zhang, Q. Zhang, and G. Cheng, "CMOS-compatible, label-free silicon-nanowire biosensors to detect cardiac troponin I for acute myocardial infarction diagnosis," *Biosensors & Bioelectronics,* vol. 34, pp. 267-272, Apr 15 2012.

[104] Z. Celik-Butler, "Low-frequency noise in deep-submicron metal-oxide-semiconductor field-effect transistors," *Circuits, Devices and Systems, IEE Proceedings -,* vol. 149, pp. 23-31, 2002.

[105] Christen.S, Lundstro.I, and C. Svensson, "Low frequency noise in MOS transistors-Theory," *Solid-State Electronics,* vol. 11, pp. 797-&, 1968 1968.

[106] B. Loncar, S. Stankovic, K. Stankovic, B. Jovanovic, and A. Electromagnet, "Influence of Gamma Radiation on Some Commercial EPROM and EEPROM Components," in *Piers 2010 Xi'an: Progress in Electromagnetics Research Symposium Proceedings, Vols 1 and 2*, ed, 2010, pp. 1193-1198.

[107] J. M. McGarrity, "Considerations for Hardening MOS Devices and Circuits for Low Radiation Doses," *Nuclear Science, IEEE Transactions on,* vol. 27, pp. 1739-1744, 1980.

[108] A. M. Kurakin, S. A. Vitusevich, S. V. Danylyuk, H. Hardtdegen, N. Klein, Z. Bougrioua*, et al.*, "Mechanism of mobility increase of the two-dimensional electron gas in AlGaN/GaN heterostructures under small dose gamma irradiation," *Journal of Applied Physics,* vol. 103, Apr 15 2008.

[109] S. Villa, G. De Geronimo, A. Pacelli, A. L. Lacaita, and A. Longoni, "Application of 1/f noise measurements to the characterization of near-interface oxide traps in ULSI n-MOSFETs," *Microelectronics Reliability,* vol. 38, pp. 1919-1923, Dec 1998.

[110] K. K. Hung, P. K. Ko, C. M. Hu, and Y. C. Cheng, "Telegraph Noise of Deep-Submicrometer MOSFET's," *Ieee Electron Device Letters,* vol. 11, pp. 90-92, Feb 1990.

[111] C. Leyris, F. Martinez, A. Hoffmann, A. Valenza, and J. C. Vildeuil, "N-MOSFET oxide trap characterization induced by nitridation process using RTS noise analysis," *Microelectronics Reliability,* vol. 47, pp. 41-45, Jan 2007.

[112] N. Lukyanchikova, M. Petrichuk, N. Garbar, E. Simoen, and C. Claeys, "RTS noise due to lateral isolation related defects in submicron nMOSFETs," *Microelectronics and Reliability,* vol. 38, pp. 1561-1568, Oct 1998.

[113] N. B. Lukyanchikova, M. V. Petrichuk, N. P. Garbar, E. Simoen, and C. Claeys, "RTS capture kinetics and Coulomb blockade energy in submicron nMOSFETs under surface quantization conditions," *Microelectronic Engineering,* vol. 48, pp. 185-188, Sep 1999.

[114] Y. Seungwon, Y. Kyoung Hwan, K. Dong-Won, S. Kang-ill, P. Donggun, J. Gyoyoung*, et al.*, "Random Telegraph Noise in n-type and p-type silicon nanowire transistors," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1-4.

[115] Y. He, S. Su, T. Xu, Y. Zhong, J. A. Zapien, J. Li*, et al.*, "Silicon nanowires-based highly-efficient SERS-active platform for ultrasensitive DNA detection," *Nano Today,* vol. 6, pp. 122-130, Apr 2011.

[116] G. Ghibaudo and O. Roux-dit-Buisson, "Low Frequency Fluctuations in Scaled Down Silicon CMOS Devices Status and Trends," in *Solid State Device Research Conference, 1994. ESSDERC '94. 24th European*, 1994, pp. 693-700.

[117] G. W. Lee, J. H. Lee, H. W. Lee, M. K. Park, D. G. Kang, and H. K. Youn, "Trap evaluations of metal/oxide/silicon field-effect transistors with high-k gate dielectric using charge pumping method," *Applied Physics Letters,* vol. 81, pp. 2050-2052, Sep 9 2002.

[118] F. Dauge, J. Pretet, S. Cristoloveanu, A. Vandooren, L. Mathew, J. Jomaah*, et al.*, "Coupling effects and channels separation in FinFETs," *Solid-State Electronics,* vol. 48, pp. 535-542, Apr 2004.

[119] Y. Yuzhelevski, M. Yuzhelevski, and G. Jung, "Random telegraph noise analysis in time domain," *Review of Scientific Instruments,* vol. 71, pp. 1681-1688, Apr 2000.

[120] H. Lee, Y. Yoon, S. Cho, and H. Shin, "Accurate extraction of the trap depth from RTS noise data by including poly depletion effect and surface potential variation in MOSFETs," *Ieice Transactions on Electronics,* vol. E90C, pp. 968-972, May 2007.

[121] E. Simoen, B. Dierickx, B. Decanne, F. Thoma, and C. Claeys, "On the Gate-Voltage and Drain-Voltage Dependence of the Rts Amplitude in Submicron Mosts," *Applied Physics a-Materials Science & Processing,* vol. 58, pp. 353-358, Apr 1994.

[122] E. Simoen, C. Claeys, N. B. Lukyanchikova, M. V. Petrichuk, and N. P. Garbar, "Single defect studies by means of random telegraph signals in submicron silicon MOSFETs," *Solid State Phenomena,* vol. 70, pp. 467-472, 1999 1999.

[123] H. H. Mueller, D. Worle, and M. Schulz, "Evaluation of the Coulomb energy for single-electron interface trapping in sub-µm metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics,* vol. 75, pp. 2970-2979, Mar 15 1994.

[124] I. P. T. V.S. Lysenko, I.N. Osiyuk, and A.N. Nazarov, Influence of traps in gate oxide-Si film transition layers on FD MOSFET's characteristics at cryogenic emperatures. Quantum Electronics & Optoelectronics 10, 34 (2007).

[125] M. Odalovic and D. Petkovic, "A model of gamma-ray irradiation effects on silicon dioxide films and on silicon dioxide-silicon interface," in *Research Trends in Contemporary Materials Science*. vol. 555, D. P. Uskokovic, S. K. Milonjic, and D. I. Rakovic, Eds., ed, 2007, pp. 147-152.

[126] Y. Huang, X. F. Duan, Y. Cui, L. J. Lauhon, K. H. Kim, and C. M. Lieber, "Logic gates and computation from assembled nanowire building blocks," *Science,* vol. 294, pp. 1313-1317, Nov 9 2001.

[127] J. Salfi, I. G. Savelyev, M. Blumin, S. V. Nair, and H. E. Ruda, "Direct observation of single-charge-detection capability of nanowire field-effect transistors (vol 5, pg 737, 2010)," *Nature Nanotechnology,* vol. 5, pp. 885-885, Dec 2010.

[128] N. B. Lukyanchikova, M. V. Petrichuk, N. P. Garbar, E. Simoen, and A. Claeys, "Impact of the free electron distribution on the random telegraph signal capture kinetics in submicron n-metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 73, pp. 2444-2446, Oct 26 1998.

[129] R. N. Hall, "Electron-Hole Recombination in Germanium," *Physical Review,* vol. 87, pp. 387-387, 1952.

[130] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Physical Review,* vol. 87, pp. 835-842, 1952.

[131] M. Schulz and A. Karmann, "Single, Individual Traps in Mosfets," *Physica Scripta,* vol. T35, pp. 273-280, 1991.

[132] M. Schulz and A. Karmann, "Individual, Attractive Defect Centers in the Sio2-Si Interface of Mu-M-Sized Mosfets," *Applied Physics a-Materials Science & Processing,* vol. 52, pp. 104-111, Feb 1991.

[133] O. Engstrom and A. Alm, "Energy Concepts of Insulator Semiconductor Interface Traps," *Journal of Applied Physics,* vol. 54, pp. 5240-5244, 1983.

[134] D. H. Cobden, M. J. Uren, and M. J. Kirton, "Entropy Measurements on Slow Si/Sio2 Interface States," *Applied Physics Letters,* vol. 56, pp. 1245-1247, Mar 26 1990.

[135] M. Schulz, " in Proceedings of the International Conference on Insulating Films on Semiconductors INFOS '93, Delft, The Netherlands, edited by P. Balk and J. J. M. de Nijs (Elsevier, Amsterdam, 1993).".

[136] M. Schulz, " in Proceedings of the International Conference on Defects in Semiconductors, Gmunden, Austria, edited by H. Heinrich (World Scientific, Singapore, 1993).".

[137] K. K. Likharev, "Correlated Discrete Transfer of Single Electrons in Ultrasmall Tunnel-Junctions," *Ibm Journal of Research and Development,* vol. 32, pp. 144-158, Jan 1988.

[138] S. Y. Chou and Y. Wang, "Single-Electron Coulomb Blockade in a Nanometer Field-Effect Transistor with a Single Barrier," *Applied Physics Letters,* vol. 61, pp. 1591-1593, Sep 28 1992.

[139] C. Schonenberger, H. Vanhouten, and H. C. Donkersloot, "Single-Electron Tunneling Observed at Room-Temperature by Scanning-Tunneling Microscopy," *Europhysics Letters,* vol. 20, pp. 249-254, Oct 1 1992.

[140] R. Berthe and J. Halbritter, "Coulomb Barriers and Adsorbate Effects in Scanning Tunneling Microscopy," *Physical Review B,* vol. 43, pp. 6880-6884, Mar 15 1991.

[141] D. A. Routenberg, "Fabrication and characterization of silicon nanowire field-effect sensors," Ph D, Yale University, 2009.

[142] M. Schulz and N. M. Johnson, "Evidence for Multiphonon Emission from Interface States in Mos Structures," *Solid State Communications,* vol. 25, pp. 481-484, 1978.

[143] D. V. Vezenov, A. Noy, L. F. Rozsnyai, and C. M. Lieber, "Force titrations and ionization state sensitive imaging of functional groups in aqueous solutions by chemical force microscopy," *Journal of the American Chemical Society,* vol. 119, pp. 2006-2015, Feb 26 1997.

[144] R. Jayaraman and C. G. Sodini, "A 1/F NOISE TECHNIQUE TO EXTRACT THE OXIDE TRAP DENSITY NEAR THE CONDUCTION-BAND EDGE OF SILICON," *Ieee Transactions on Electron Devices,* vol. 36, pp. 1773-1782, Sep 1989.

[145] S. Sorgenfrei, C. Y. Chiu, R. L. Gonzalez, Jr., Y. J. Yu, P. Kim, C. Nuckolls*, et al.*, "Label-free single-molecule detection of DNA-hybridization kinetics with a carbon nanotube field-effect transistor," *Nat Nanotechnol,* vol. 6, pp. 126-32, Feb 2011.

[146] S. Sorgenfrei, C. Y. Chiu, M. Johnston, C. Nuckolls, and K. L. Shepard, "Debye screening in single-molecule carbon nanotube field-effect sensors," *Nano Lett,* vol. 11, pp. 3739-43, Sep 14 2011.

[147] Y. Choi, T. J. Olsen, P. C. Sims, I. S. Moody, B. L. Corso, M. N. Dang*, et al.*, "Dissecting single-molecule signal transduction in carbon nanotube circuits with protein engineering," *Nano Lett,* vol. 13, pp. 625-31, Feb 13 2013.

[148] J. Liu, C. Xie, X. Dai, L. Jin, W. Zhou, and C. M. Lieber, "Multifunctional three-dimensional macroporous nanoelectronic networks for smart materials," *Proc Natl Acad Sci U S A,* vol. 110, pp. 6694-9, Apr 23 2013.

[149] N. K. Rajan, D. A. Routenberg, and M. A. Reed, "Optimal signal-to-noise ratio for silicon nanowire biochemical sensors," *Appl Phys Lett,* vol. 98, pp. 264107-2641073, Jun 27 2011.

[150] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, 3rd ed. Hoboken, N.J.: Wiley-Interscience, 2007.

[151] T. A. Fjeldly and M. Shur, "Threshold Voltage Modeling and the Subthreshold Regime of Operation of Short-Channel Mosfets," *Ieee Transactions on Electron Devices,* vol. 40, pp. 137-145, Jan 1993.

[152] S. R. Banna, P. C. H. Chan, P. K. Ko, C. T. Nguyen, and M. S. Chan, "Threshold Voltage Model for Deep-Submicrometer Fully Depleted Soi Mosfets," *Ieee Transactions on Electron Devices,* vol. 42, pp. 1949-1955, Nov 1995.

[153] Z. H. Liu, C. M. Hu, J. H. Huang, T. Y. Chan, M. C. Jeng, P. K. Ko*, et al.*, "Threshold Voltage Model for Deep-Submicrometer Mosfets," *Ieee Transactions on Electron Devices,* vol. 40, pp. 86-95, Jan 1993.

[154] C. Q. Wei, Y. Z. Xiong, and X. Zhou, "Investigation of Low-Frequency Noise in N-Channel FinFETs From Weak to Strong Inversion," *Ieee Transactions on Electron Devices,* vol. 56, pp. 2800-2810, Nov 2009.

[155] D. H. Cobden and B. A. Muzykantskii, "Finite-Temperature Fermi-Edge Singularity in Tunneling Studied Using Random Telegraph Signals," *Physical Review Letters,* vol. 75, pp. 4274-4277, Dec 4 1995.

[156] J. Li, S. Pud, M. Petrychuk, A. Offenhausser, and S. Vitusevich, "Sensitivity Enhancement of Si Nanowire Field Effect Transistor Biosensors Using Single Trap Phenomena," *Nano Letters,* vol. 14, pp. 3504-3509, Jun 2014.

[157] G. H. Bolt, "Determination of the Charge Density of Silica Sols," *Journal of Physical Chemistry,* vol. 61, pp. 1166-1169, 1957.

Publications list

[1] J. Li, S. Pud, D. Mayer, and S. Vitusevich, "Advanced fabrication of Si nanowire FET structures by means of a parallel approach," *Nanotechnology,* vol. 25, Jul 11 2014.

[2] S. Pud, F. Gasparyan, M. Petrychuk, J. Li, A. Offenhausser, and S. A. Vitusevich, "Single trap dynamics in electrolyte-gated Si-nanowire field effect transistors," *Journal of Applied Physics,* vol. 115, Jun 21 2014.

[3] J. Li, S. Pud, M. Petrychuk, A. Offenhausser, and S. Vitusevich, "Sensitivity Enhancement of Si Nanowire Field Effect Transistor Biosensors Using Single Trap Phenomena," *Nano Letters,* vol. 14, pp. 3504-3509, Jun 2014.

[4] S. Pud, J. Li, V. Sibiliev, M. Petrychuk, V. Kovalenko, A. Offenhausser*, et al.*, "Liquid and Back Gate Coupling Effect: Toward Biosensing with Lowest Detection Limit," *Nano Letters,* vol. 14, pp. 578-584, Feb 2014.

[5] V. A. Sydoruk, K. Goss, C. Meyer, M. V. Petrychuk, B. A. Danilchenko, P. Weber, C. Stampfer, J. Li and S. A. Vitusevich, "Low-frequency noise in individual carbon nanotube field-effect transistors with top, side and back gate configurations: effect of gamma irradiation," *Nanotechnology,* vol. 25, Jan 24 2014.

[6] J. Li, S. A. Vitusevich, M. V. Petrychuk, S. Pud, A. Offenhausser, and B. A. Danilchenko, "Advanced performance and scalability of Si nanowire field-effect transistors analyzed using noise spectroscopy and gamma radiation techniques," *Journal of Applied Physics,* vol. 114, Nov 28 2013.

[7] S. Pud, J. Li, M. Petrychuk, S. Feste, S. Vitusevich, B. Danilchenko*, et al.*, "Modulation phenomena in Si nanowire field-effect transistors characterized using noise spectroscopy and gamma radiation technique," *Journal of Applied Physics,* vol. 113, Mar 28 2013.

[8] S. Vitusevich, J. Li, S. Pud, A. Offenhaeusser, M. Petrychuk, and B. Danilchenko, "Si Nanowire Field Effect Transistors: Effect of Gamma Radiation Treatment," *2013 22nd International Conference on Noise and Fluctuations (Icnf),* 2013.

[9] S. Richter, S. Vitusevich, S. Pud, J. Li, L. Knoll, S. Trellenkamp*, et al.*, "Low Frequency Noise in Strained Silicon Nanowire Array MOSFETs and Tunnel-FETs," *2013 Proceedings of the European Solid-State Device Research Conference (Essderc),* pp. 256-259, 2013.

[10] S. Pud, J. Li, V. Sibiliev, A. Acevedo, M. Petrychuk, A. Offenhausser*, et al.*, "Noise and Transport Characteristics of Silicon Nanowire Field Effect Transistors with Liquid Gate," *2013 22nd International Conference on Noise and Fluctuations (Icnf),* 2013.

[11] J. Li, S. Vitusevich, M. Petrychuk, S. Pud, V. Sydoruk, B. Danilchenko*, et al.*, "Transport and Noise Properties of Si Nanowire Channels with Different Lengths

Before and After Gamma Radiation Treatment," *Physics of Semiconductors,* vol. 1566, pp. 389-390, 2013.

[12] A. V. Sachenko, A. E. Belyaev, N. S. Boltovets, R. V. Konakova, Y. Y. Kudryk, S. V. Novitskii, V. N. Sheremet, J. Li and S. A. Vitusevich, "Mechanism of contact resistance formation in ohmic contacts with high dislocation density," *Journal of Applied Physics,* vol. 111, Apr 15 2012.

[13] S. Pud, J. Li, M. Petrychuk, S. Feste, A. Offenhausser, S. Mantl*, et al.*, "Noise Spectroscopy of Traps in Silicon Nanowire Field-Effect Transistors," *2011 21st International Conference on Noise and Fluctuations (Icnf),* pp. 242-245, 2011.

Appendixes

A. Nanoimprint Mold Fabrication

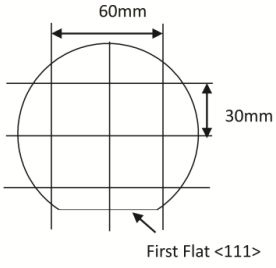
A.1. Starting with Si<110> substrate

Company	Si-Mat Silicon Materials
Growth method	CZ
Diameter	100.0 +/- 0.5 mm
Type of conductivity	P
Dopant	Boron
Surface orientation	<1-1-0>
Thickness	525+/-25 µm
Resistivity	3 - 10 ohm
Primary flat position	<111> plane

A.2. Dry oxidation

Parameter	Time	Temperature	Thickness
Wet oxidation	3 min	1050 °C	115 nm

A.3. Wafer cutting



Wafer diameter	100 mm
Elements square	30 × 30 mm^2

A.4. PMMA spincoating

1	Pre bake	180 °C, 5 min
or	HMDS	
2	PMMA 600K (AR-P669.04)	500 rpm/30 sec and 4000 rpm/30 sec
3	Soft bake (vacuum)	180 °C /2 min

A.5. E-beam writing and development.

i. E-beam writing

E-beam parameter	Dose ($\mu C/cm^2$)	E-beam current (nA)	Beam step size (nm)
Conducting lane(Coarse pattern dose)	225	150	50
Nanowire (Fine pattern dose)	380	1	5

ii. Development

Development (megasonic)	Solvent	Time (s)
1	AR 600-55	45
2	Isopropanole	30

A.6. RIE etching: SiO_2 and PMMA

1	PMMA residual layer	O_2 plasma	3 sec
2	SiO_2 layer	CHF_3 plasma	5 min
3	PMMA	O_2 plasma	1 min

A.7. KOH etching: Si

1	SiO_2 native oxide layer	1% HF	20 sec
2	Si	KOH (20%, 30 °C)	150-200 nm

A.8. HF (10%) etching: SiO_2

10% HF etching for 20 sec to remove the residual SiO_2 layer

SiO_2	HF (10%) Etching rate	Needed time	Used time
115 nm	23 nm/min	5 min 26 sec	6 min

A.9. Silanization

The fabricated mold was passivated by covalently linking a trichloro(1H,1H,2H,2H-perfluorooctyl)silane (FOTS) monolayer which has a functional unit of-CF_3 as an anti-adhesion layer on the mold by a vapor deposition process.

B. Chip Fabrication

B.1. Fabrication of Back Gate Si NW FETs with Micrometer Channels

B.2.1. Imprint mold (3 × 3 mm^2 and 5 × 5 mm^2)

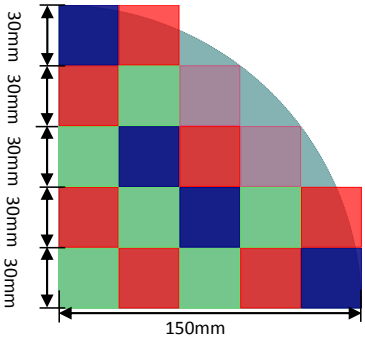
Nanoimprint mold were fabricated by EBL and RIE.

B.2.2. Starting wafer

SOI, Si (70 nm)/SiO_2 (145 nm)

Top silicon	Layer thickness	70 nm
	Doping type	P-Type
	Crystal orientation	(100)
Buried Oxide (BOX)	Thickness	145 nm
Primary flat position	<111> plane	

B.2.3. Wafer cutting



Wafer diameter	300 mm
Elements square	30 × 30 mm^2

B.2.4. RCA cleaning

B.2.5. Dry oxidation

Dry oxidation parameter	Time	Temperature	Thickness	Active layer

Dry oxidation	30 min	1000 °C	37 nm	54 nm

B.2.6. Thermal nanoimprint

i. Nanoimprint resist spincoating

1	Pre bake	180 °C, 5 min
2	NXR-1025 Nanoimprint Resist	3000 rpm, 30 sec
3	Soft bake (vacuum)	90 °C, 20 min

ii. Thermal nanomprint

1	Before imprint process	5 min
2	Pre imprint	350 PSI, 120 °C.
3	Imprint process	550 PSI, 160 °C, 6 min
4	Demolding temperature	35 °C

B.2.7. RIE etching residual layer and SiO_2 layer

i. Nanowires region etching

1	Residual layer	O_2 plasma	15 sec
2	SiO_2 layer	CHF_3 plasma	1 min 15 sec
3	Resist	O_2 plasma	1 min

ii. Edge region etching

1	Lithography	AZ5214	
2	SiO_2 layer	CHF_3 plasma	1 min 30 sec
3	Remove resist	Acetone+isopropanol	

B.2.8. TMAH etching to define Si NW structures

1	Before TMAH etching	20 sec in HF 1%
2	Rinse by DI Water	Dry under N_2 flow
3	TMAH etching	TMAH 25%, 90 °C, 1 min

B.2.9. Oxidation layer

Dry oxidation	30 min	850 °C	8 nm

B.2.10. Ion implantation protection layer

Lithography	AZ5214

B.2.11. Ion implantation

Ion	Ion implantation (As)
Energy	8 Kev, 7 degree, 5 x $10^{14}/cm^2$
Activation	Activation of was carried out by RTA at 950 °C for 30 sec in N_2 atmosphere.

B.2.12. Cleaning

1	O_2 plasma	30 sec
2	Aceton	Half a day
3	Piranha cleaning	Two times

B.2.13. Mask layer removing

HF 1% 6 min

B.2.14. RCA cleanring

B.2.15. Oxidation layer

Dry oxidation	30 min	850 °C	8 nm
PECVD (SiO_2)	4 min	350 °C	94 nm

B.2.16. Back gate opening

1	Lithography	AZ5214	
2	Residual layer	O_2 plasma	3 sec
3	SiO_2 layer (145 nm)	CHF_3 plasma	6 min
4	Resist	O_2 plasma	1 min

B.2.17. Contact pad opening

1	Lithography	AZ5214	
2	Residual layer	O_2 plasma	10 sec
3	SiO_2 layer (300 nm)	CHF_3 plasma	30 sec
4	Resist	O_2 plasma	5-10 min

B.2.18. Lift-off

1	Lithography	AZ5214
2	Ar sputtering	20 sec/300 W
3	Al/Ti/Au sputtering	150 nm/10 nm/150 nm
4	Lift -off	Acetone+isopropanol

B.2. Fabrication of Back Gate Si NW FETs with Submicrometer Channels

B.2.1. Molds

Nanoimprint mold were fabricated by EBL and RIE

B.2.2. Starting wafer

SOI, Si (70 nm)/SiO_2 (145 nm)

B.2.3. Wafer cutting

Wafer diameter	300 mm
Elements square	30 × 30 mm^2

B.2.4. RCA cleaning

B.2.5. Dry oxidation

Dry oxidation parameter	Time	Temperature	Thickness	Active layer
Dry oxidation	30 min	1000 °C	37 nm	54 nm

B.2.6. Thermal nanoimprint

i. Nanoimprint resist spincoating

1	Pre bake	180 °C, 5 min
2	NXR-1025 Nanoimprint Resist	6000 rpm, 30 sec
3	Soft bake (vacuum)	Vacuum

ii.Thermal imprinting

1	Before imprint process	5 min
2	Pre imprint	350 PSI, 120 °C

3	Imprint process	550 PSI, 160 °C, 6 min
4	Demolding temperature	35 °C

B.2.7. RIE etching residual layer and SiO_2 layer

1	Residual layer	O_2 plasma	30 sec
2	SiO_2 layer	CHF_3 Ar plasma	1 min 30 sec
3	Resist	O_2 plasma	1 min

B.2.8. TMAH etching to define Si NW Structures

1	Before TMAH etching	20 sec in HF 1%
2	Rinse by DI Water	Dry under N_2 flow
3	TMAH etching	TMAH 25%, 90 °C, 30 sec

B.2.9. RCA cleanning

B.2.10. Dry oxidation (RTP)

Dry oxidation	6 min	1000 °C	8.5 nm

B.2.11. Ion implantation protection layer

i. HSQ resist coating

1	Pre bake	180 °C, 5 min
2	HSQ resist	6000 rpm, 30 sec
3	Low temperature bake	150 °C, 2 min
4	High temperature bake	220 °C, 2 min

ii. E-beam writing

E-beam parameter	Dose ($\mu C/cm^2$)	E-beam current (nA)	Beam step size (nm)
protection pattern	1100	1	5

iii. Development process: 1min or more

B.2.12. Implantation (5 nm SiO_2/50 nm Si/145 nm SiO_2)

Ion	Ion implantation (As)
Energy	10 Kev, 7 degree, 5 x $10^{14}/cm^2$
Activation	Activation of was carried out by RTA at 950 °C for 30 sec in N_2 atmosphere.

B.2.13. Cleaning

1	O_2 plasma	30 sec
2	Acetone	Half a day
3	Piranha cleaning	2 times

B.2.14. PECVD passivation

PECVD	Thickness
SiO_2	100 nm

B.2.15. Back Gate opening

1	Lithography	AZ5214	
		Hard baking/115 °C	5 min
2	SiO_2 layer 145 nm+100 nm SiO_2 PECVD	BHF 125-875	5 min

3	Resist	Aceton	Half a day
		Piranha cleaning	

B.2.16. Contact pad opening

1	Lithography	AZ5214	
		Hard baking/115 °C	5 min
2	SiO_2 layer (100 nm)	HF (1%)	5 min
3	Resist	Aceton	Half a day
		Piranha cleaning	

B.2.17. Lift-off

1	Lithography	LOR 3B / 3000 rpm	180 °C/ 5 min
		nlof/3000 rpm	110 °C/ 1 min
2	Ar sputtering	10 sec/300 W	
3	Al sputtering	200 nm	
4	Lift -off	EBR PG	1 night
		Acetone + isopropanol	

B.2.18. Annealing (400 °C /10 min) RTP oven, N_2, H_2 forming gas form ohmic contact.

B.3. Si NW FET Biosensor Fabricated by T-NIL with Micrometer Channels

B.3.1. Molds

SiO_2/Si mold by EBL and RIE

B.3.2. Starting wafer

SOI, Si (70 nm)/SiO_2 (145 nm)

B.3.3. Wafer cutting

Wafer diameter	300 mm
Elements square	30 × 30 mm^2

B.3.4. RCA cleaning

B.3.5. Growth of 30 nm SiO_2

Using dry oxidation to get SiO_2 with a thickness of 30 nm

Dry oxidation parameter	Time	Temperature	Thickness	Active layer
dry oxidation	30 min	1000 °C	37 nm	54 nm

B.3.6. Thermal nanoimprint

i. Nanoimprint resist coating

1	Pre bake	180 °C, 5 min
2	NXR-1025 Nanoimprint Resist	4000 rpm, 30 sec
3	Soft bake (vacuum)	Vacuum

ii. Thermal Imprint

1	Before imprint process	5 min
2	Pre imprint	350 PSI, 120 °C

3	Imprint process	550 PSI, 160 °C, 6 min
4	Demolding temperature	35 °C

B.3.7. RIE etching residual layer and SiO_2 layer

1	Residual layer	O_2 plasma	30 sec
2	SiO_2 layer	CHF_3, Ar plasma	1 min 30 sec
3	Resist	O_2 plasma	1 min

B.3.8. TMAH etching to define Si NW Structure

1	before TMAH etching	20 sec in HF 1%
2	Rinse by DI Water	dry under N_2 flow
3	TMAH etching	TMAH 25%, 90 °C, 30 sec

B.3.8. Mask layer removing

HF 1% 6 min

B.3.9. RCA cleanring

B.3.10. Dry oxidation (RTP)

Dry oxidation (RTP)	2 min	1000 °C	5 nm

B.3.11. Back gate opening

1	Lithography	AZ5214	
		Hard baking/115 °C	5 min
2	SiO_2 layer 145 nm + 100 nm SiO_2 PECVD	BHF 125-875	5 min

3	Resist	Aceton	Half a day
4		Piranha cleaning	

B.3.12. Ion implantation protection layer

Lithography	AZ5214

B.3.13. Implantation (SiO_2 (5 nm)/Si (50 nm)/SiO_2 (145 nm))

Ion	Ion implantation (B)	Ion implantation (As)
Energy	7Kev, 7degree, 1 x $10^{15}/cm^2$	20Kev, 7degree, 1 x $10^{15}/cm^2$
Activation	Activation was carried out by RTA at 1000 °C for 5 sec in N_2 atmosphere.	Activation of was carried out by RTA at 950 ℃ for 30 sec in N_2 atmosphere.

B.3.14. Cleaning

1	O_2 plasma	30 sec
2	Aceton	Half a day
3	Piranha cleaning	Two times
4	HF 1%	2-3 min
5	RCA cleanring	

B.3.15. Dry oxidation (RTP)

Dry oxidation (RTP)	8 min	1000 ℃	8 nm

B.3.16. ALD

ALD	Thickness

Al_2O_3	6 nm

B.3.15. Contact pad opening

1	Lithography	AZ5214	
2		Hard baking/115 °C	5 min
3	Al_2O_3 (ALD, 6nm) etching	H_3PO_4/ 50 °C	5 min
4	SiO_2 layer (8nm)	1% HF	2 min
5	Resist	Aceton	One night

B.3.16. Lift-off

i. Resist spinning

1	Water removing	180 °C, 5 min
2	LOR 3B 3000 rpm	180 °C, 5 min
3	nlof 2020 3000 rpm	110 °C, 1 min
4	Post exposure baking	110 °C, 1 min 30sec
5	MIF326	45 sec
6	DI water	5 min

ii. Metal sputtering

1	Ar Sputtering	30 sec
2	Al/Ti/Au 150/10/150 nm	
3	EBR PG	1 night
4	Aceton + isopropanol	

B.3.17. Annealing

RTP (400 °C/10 min), N_2/H_2 forming gas form ohmic contact.

B.3.18. Passivation layer

1	5 min/180°	
2	SU8-2 / 4000 rpm	60 °C /1 min + 95 °C/1min
3	Exposure	3 sec, 7 mW/cm^2
4	Post exposure baking	60 °C /1 min + 95 °C/1 min
5	Development	1 min
6	hard baking	180 °C, 30 min

B.4. Si NW FET Biosensor Fabricated by EBL with Submicrometer Channels

B.4.1. Starting wafer

SOI, Si (70 nm)/SiO_2 (145 nm).

B.4.2. Wafer cutting

Wafer diameter	300 mm
Elements square	30 × 30 mm^2

B.4.3. RCA cleaning

B.4.4. Dry oxidation

Dry oxidation parameter	Time	Temperature	Thickness	Active layer
Dry oxidation	30 min	1000 °C	37 nm	54 nm

B.4.5. Oxide layer thinning

HF etching	Time	Thickness	Active layer
SOI/SiO_2	5 min	15 nm	54 nm

B.4.6. HSQ resist coating

1	Pre bake	180 °C, 5 min
2	HSQ resist	6000 rpm, 30 sec
3	Low temperature bake	150 °C, 2 min
4	High temperature bake	220 °C, 2 min

B.4.7. E-beam writing (with proximity effect correction)

E-beam parameter	Dose ($\mu C/cm^2$)	E-beam current (nA)	Beam step size (nm)
Conducting lane (Coarse pattern dose)	300	150	50
Nanowire (Fine pattern dose)	300	0.2	2

B.4.8. Development

Develop: MF-CD-26A, 60secs; water rinse 30s, N_2 blow dry.

B.4.9. RIE etching

1	Residual layer	O_2 plasma	30 sec
2	SiO_2 layer	CHF_3 Ar plasma	45 sec
3	Resist	O_2 plasma	30 sec

B.4.10. TMAH etching to define Si NW Structures

1	Before TMAH etching	10 sec in HF 1%
2	Rinse by DI Water	Dry under N_2 flow
3	TMAH etching	TMAH 25%, 90 °C, 30 sec

B.4.11. Mask layer removing

HF 1% 4 min

B.4.12. RCA cleanring

B.4.13. Dry oxidation (RTP)

Dry oxidation	2 min	1000 °C	4.6 nm

B.4.14. Ion implantation protect layer

i. HSQ resist coating

1	Pre bake	180 °C, 5 min
2	HSQ resist	6000 rpm, 30 sec
3	Low temperature baking	150 °C, 2 min
4	High temperature baking	220 °C, 2 min

ii. E-beam writing

E-beam parameter	Dose ($\mu C/cm^2$)	E-beam current (nA)	Beam step size (nm)
protection pattern	1100	1	5

iii. Development process: 1 min or more

B.4.15. Back Gate opening

1	Lithography	AZ5214	
		Hard baking/115 °C	5 min
2	SiO_2 layer 145 nm + 100 nm SiO_2 (PECVD)	BHF 125-875	5 min
3	Resist	Aceton	Half a day
		Piranha cleaning	

B.4.16. Implantation (5 nm SiO_2/50 nm Si/145 nm SiO_2)

Ion	Ion implantation (B)	Ion implantation (As)
Energy	7 Kev, 7 degree, 1 x $10^{15}/cm^2$	20 Kev, 7degree, 1 x $10^{15}/cm^2$
Activation	Activation of BF_2 was carried out by RTA at 1000 °C for 5 sec in N_2 atmosphere.	Activation was carried out by RTA at 950 °C for 30 sec in N_2 atmosphere.

B.4.17. Contact pad opening

1	Lithography	AZ5214	
		Hard baking/115 °C	5 min
2	SiO_2 layer(100 nm)	HF (1%)	5 min
4	Resist	Aceton	Half a day
		Piranha cleaning	

B.4.18. RCA cleanring

B.4.19. Dry oxidation (RTP)

Dry oxidation	6 min	1000 °C	8.5 nm

B.4.20. Lift-off

1	Lithography	LOR 3B/3000 rpm	180 °C / 5 min
		nlof/3000 rpm	110 °C / 1 min
2	Ar sputtering	10 sec/300 W	
3	Al sputtering	200 nm	
4	Lift -off	EBR PG	1 night

B.4.21. Annealing (400 °C/10 min) RTP oven, N_2/H_2 forming gas form ohmic contact.

C. Abbreviations

AFM	Atomic force microscopy
APTES	3-aminopropyl-triethoxysilane
BOX	Buried oxide
BG	Back gate
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
CNTFETs	Carbon nanotube field effect transistor
D	Drain
DNA	Deoxyribonucleic acid
DUV	Deep UV lithography
DIBL	Drain induced barrier lowering effect
EBL	Electron-beam lithography
FET	Field effect transistor
FIB	Focused ion beam
FG	Front gate
FOTS	Trichloro(1H,1H,2H,2H-perfluorooctyl)silane
G	Gate
G-R	Generation-recombination
HF	Hydrofluoric acid

C. Abbreviations

HSQ	Hydrogen silsesquioxane
ISFET	Ion sensitive field effect transistor
ITRS	International Technology Roadmap for Semiconductors
I-V	Current- voltage
PECVD	Plasma enhanced chemical vapor deposition
PSD	Power spectral density
MOSFET	Metal oxide semiconductor field effect transistor
NIL	Nanoimprint lithography
NW	Nanowire
PBS	Phosphate Buffered Saline
PMMA	Poly(methyl methacrylate)
RE	Reference electrode
RIE	Reactive ion etching
RTP	Rapid thermal processing
RTS	Random telegraph signal
S	Source
Si NW	Silicon nanowire
SEM	Scanning electron microscope
SOI	Silicon-on-Insulator
SNR	Signal-to-noise ratio

SRH	Shockley Read Hall
T-NIL	Thermal nanoimprint lithography
TMAH	Tetramethylammonium hydroxide
TEM	Transmission electron microscope
UV-NIL	UV nanoimprint lithography
VLS	Vapor-liquid-solid

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